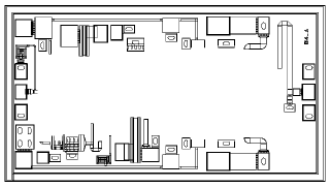
AMT1112
8 – 12GHz Power Amplifier Chip



Key Features :

- Frequency range : 8 – 12GHz
- Typical small signal gain : 28dB
- Typical output power : 35.5dBm
- Typical power added efficiency (PAE) : 40%
- Voltage Bias : 8V, -0.7V
- Chip dimensions : 2.8mm x 1.5mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1112 chip is designed by Gallium Arsenide (GaAs) pHEMT process, a high performance 8 - 12GHz power amplifier, it uses dual voltage operation, with drain voltage Vds at 8.0V, it offers 35dBm power output in the frequency range of 8 – 12GHz. This chip is designed with ground through metal vias on the back technology. All chip products are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	9V	
Id	Drain Current	2A	
Vg	Gate Voltage	-0.5V	
Ig	Gate Current	50mA	
Pd	Power Dissipation	16W	
Pin	Input Signal Power	25dBm	
Tch	Operating Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

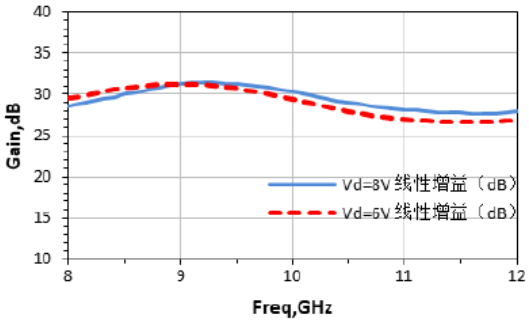
Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Test Condition	Value			Unit
			Min	Typical	Max	
G	Small Signal Gain	Vd = 8V Vg = -0.7V F : 8 ~ 12GHz	25	28	-	dB
VSWRi	Input Standing Wave		-	1.8	2	
Pout	Saturated Power Output		34.5	35.5	36.5	dBm
PAE	Power Added Efficiency		38	40	-	%
I_D	Dynamic Current		-	1.2	1.3	A
I_J	Static Current		-	1	1.1	A

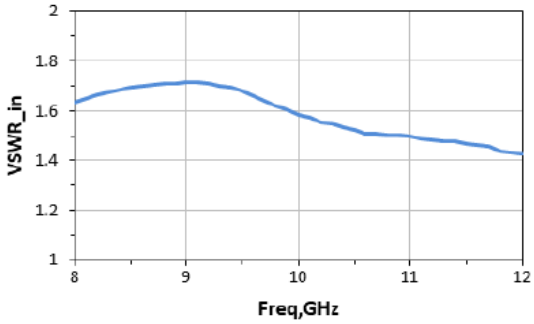
Note, no CW operation.

Typical Performance

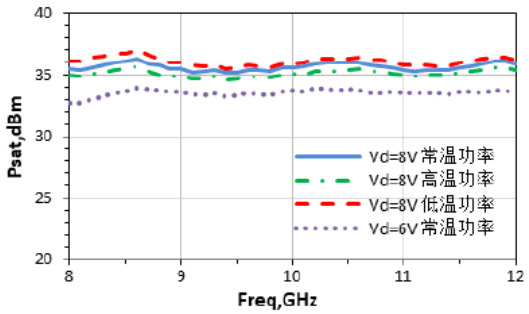
Gain Curve



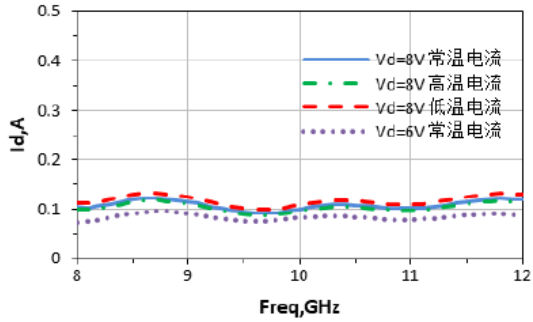
Input Standing Wave Curve



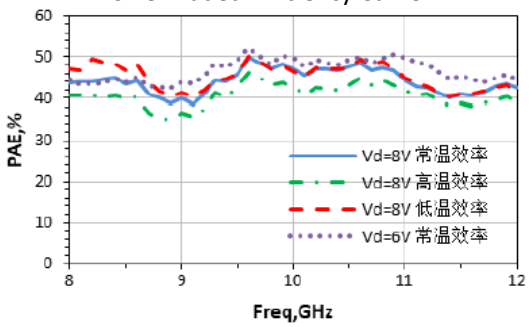
Saturated Output Power Curve



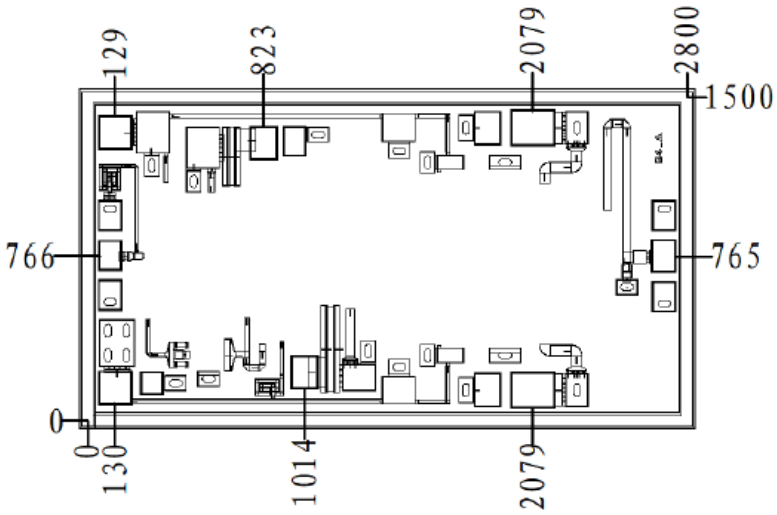
Current Curve



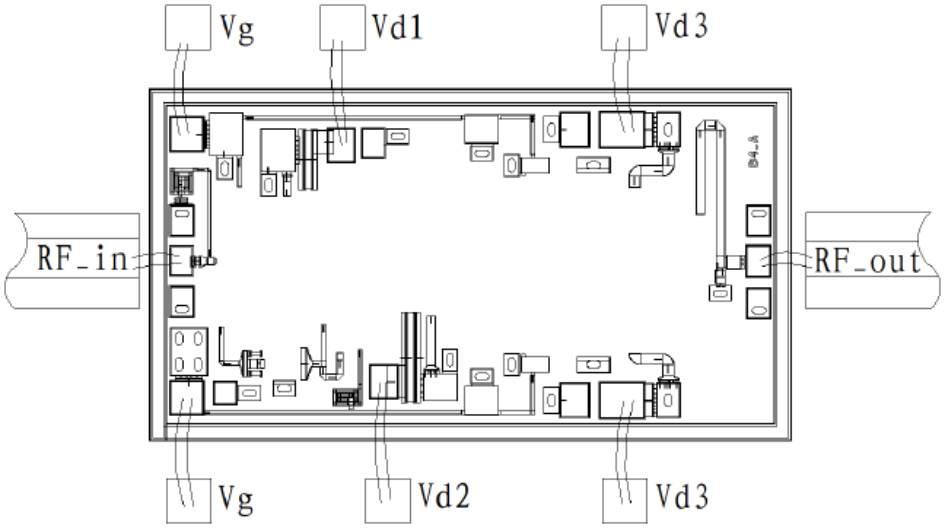
Power Added Efficiency Curve



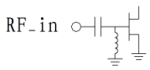
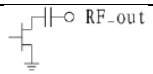
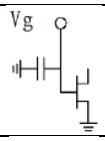
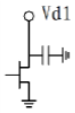
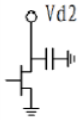
Chip Dimensions (Unit : μm)



Chip Layout Diagram



Pad Definition

Symbol	Function	Dimension	Equivalent Circuit
RF_in	RF signal input port, connecting to external 50Ω system. DC blocking capacitor is needed, if external DC current is applied to this pad.	100*128μm^2	
RF_out	RF signal output port, connecting to external 50Ω system, no need to add DC blocking capacitor.	110*138μm^2	
Vg	Amplifier gate bias, need external 100pF, 1000pF capacitor.	150*150μm^2	
Vd1	Amplifier drain bias, need external 100pF, 1000pF capacitor.	120*150μm^2	
Vd2	Amplifier drain bias, need external 100pF, 1000pF capacitor.	120*150μm^2	
Vd3	Amplifier drain bias, need external 100pF, 1000pF capacitor.	200*160μm^2	

Please see Appendix A for details.