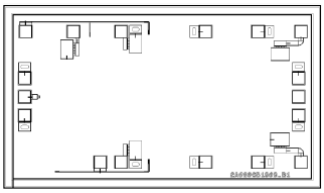
AMT1115

13 – 18GHz Power Amplifier Chip



Key Features :

- Frequency range : 13 – 18GHz
- Typical small signal gain : 22dB
- Typical output power : 33.5dBm
- Voltage bias : Vd = 8V, Vg = -0.6V
- Chip dimensions : 2.5mm x 1.4mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1115 chip is a Gallium Arsenide (GaAs) designed high performance power amplifier for 16 - 28GHz frequency range. It uses dual voltage operation, with drain voltage Vds at 8V, it offers 22dB linear gain, and 33.5dBm saturated output power. This chip is designed with ground through metal vias on the back technology. All chip products are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	+11V	
Pin	Input Signal Power	15dBm	
Tch	Operating Temperature	175°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

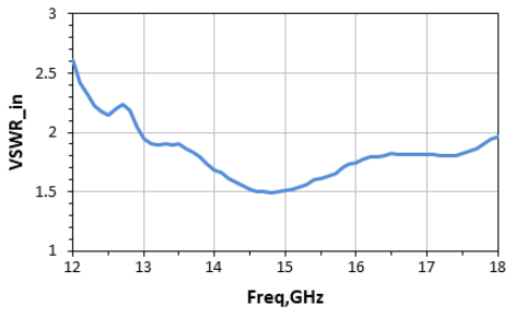
Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Test Condition	Value			Unit
			Min	Typical	Max	
G	Small Signal Gain	Vd = 8V, Vg=-0.6V F : 13 ~ 18GHz	21	22	26	dB
Id	Operation Current		-	1.1	-	A
VSWR_in	Input SW		-	1.8	1.9	-
VSWR_out	Output SW		-	1.3	1.5	-
Gp	Power Gain	Vd = 8V, Vg=-0.6V F : 13 ~ 18GHz Duty Cycle : 20%	-	23.5	-	dB
Po(sat)	Saturated Output Power		-	33.5	-	dBm
PAE	Power Added Efficiency		-	30	-	%

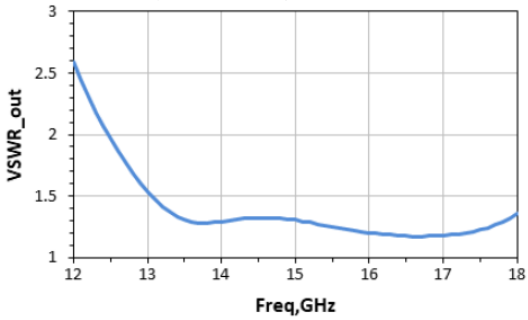
Note, no CW operation.

Typical Performance

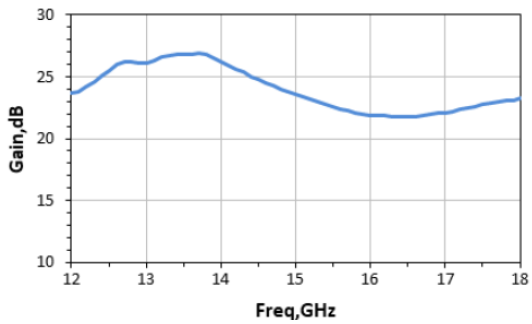
Input Standing Wave Curve



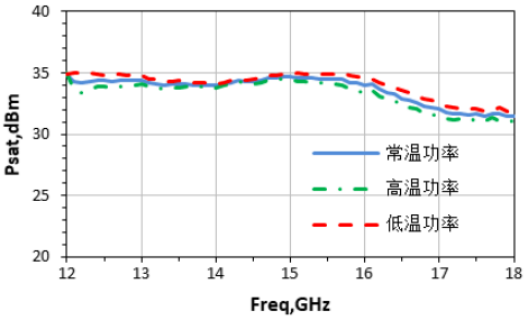
Output Standing Wave Curve



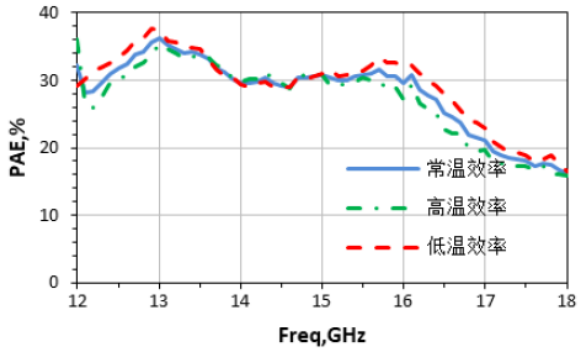
Gain Curve



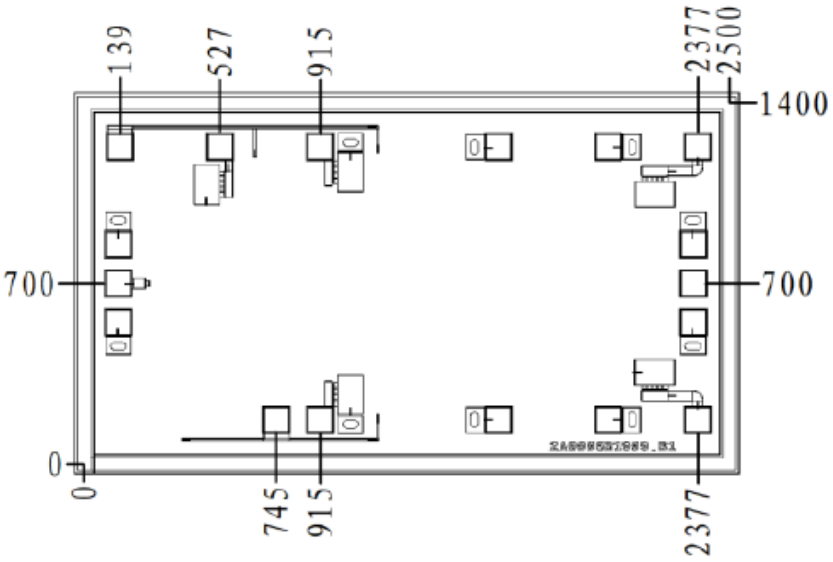
Output Power Curve



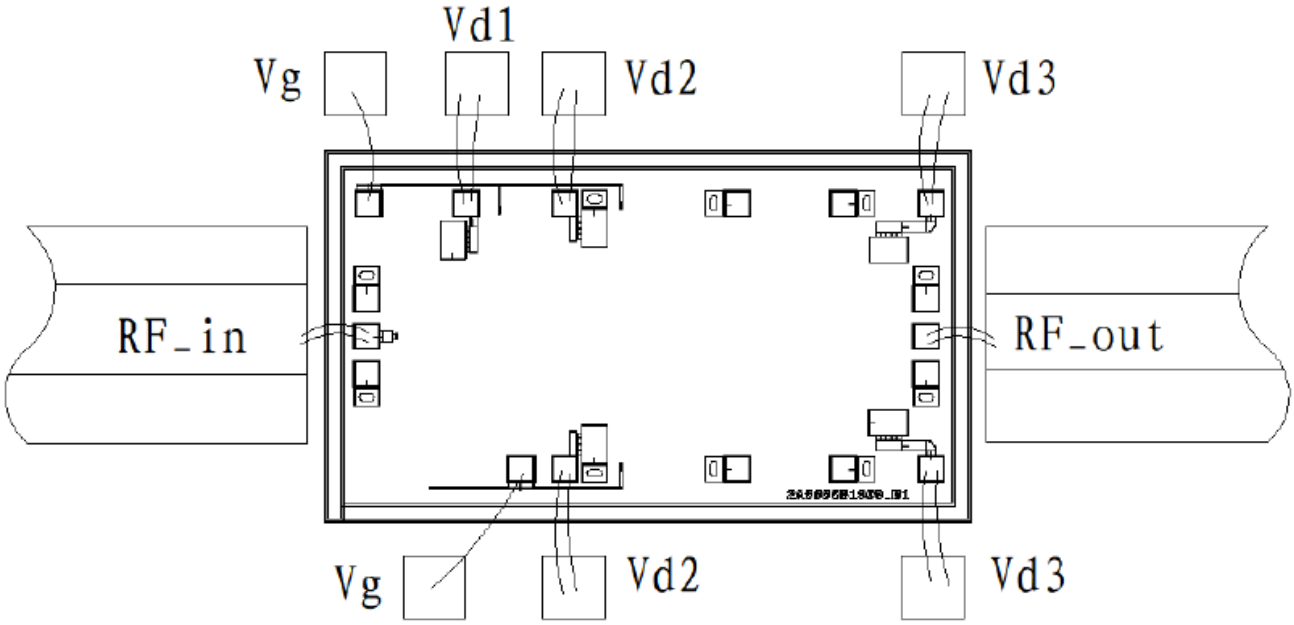
Power Added Efficiency Curve



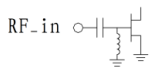
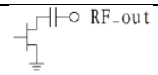
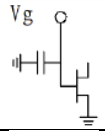
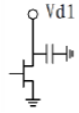
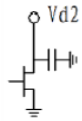
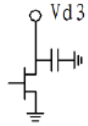
Chip Dimensions (Unit : μm)



Chip Layout Diagram



Pad Definition

Symbol	Function	Dimension	Equivalent Circuit
RF_in	RF signal input port, connecting to external 50Ω system. DC blocking capacitor is not needed, if external DC current is applied to this pad.	100*100μm^2	
RF_out	RF signal output port, connecting to external 50Ω system, no need to add DC blocking capacitor.	100*100μm^2	
Vg	Amplifier gate bias, need external 100pF, 1000pF capacitor.	100*100μm^2	
Vd1	Amplifier drain bias, need external 100pF, 1000pF capacitor.	100*100μm^2	
Vd2	Amplifier drain bias, need external 100pF, 1000pF capacitor.	100*100μm^2	
Vd3	Amplifier drain bias, need external 100pF, 1000pF capacitor.	100*100μm^2	

Please see Appendix A for details.