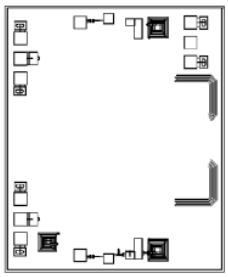
AMT1211

7 – 13GHz Low Noise Amplifier Chip



Key Features :

- Frequency range : 7 – 13GHz
- Typical gain : 25dB
- Input/output standing wave : 1.3
- Noise figure : 1.5dB
- P-1 : 13dBm @ +5V/32mA
- Chip dimensions : 2mm x 1.65mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1211 chip is a Gallium Arsenide (GaAs) high performance Low Noise Amplifier, it covers 7 – 13GHz frequency range. It uses +5V single voltage operation, Noise Figure is 1.5dB, and 25dB typical gain. This chip is designed with ground through metal vias on the back technology. All chip products p are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	7V	
Pin	Input Signal Power	17dBm	
Tch	Operating Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

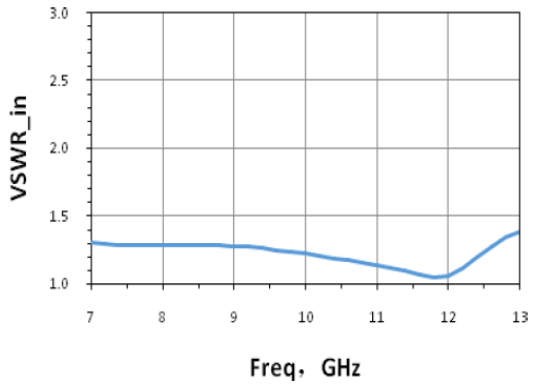
[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

Electrical Characteristics (Ta = 25°C)

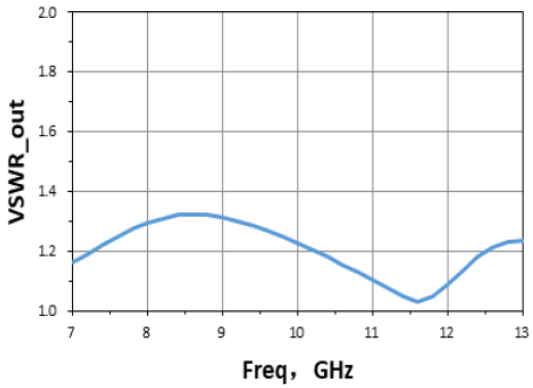
Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typical	Max	
G	Gain	Vd = +5V F : 7 ~ 13GHz	24	25	-	dB
NF	Noise Figure		-	1.5	2	dB
Id	Static Current		-	32	45	mA
VSWR_in	Input Standing Wave		-	1.3	1.6	
VSWR_out	Output Standing Wave		-	1.3	1.6	
P-1	Output Power at 1dB point		9	13	-	dBm

Typical Performance

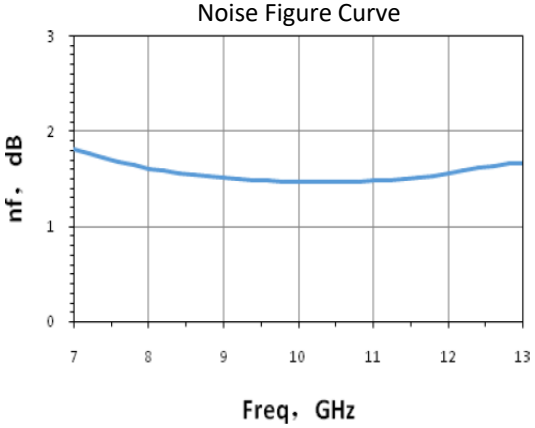
Input Standing Wave Curve



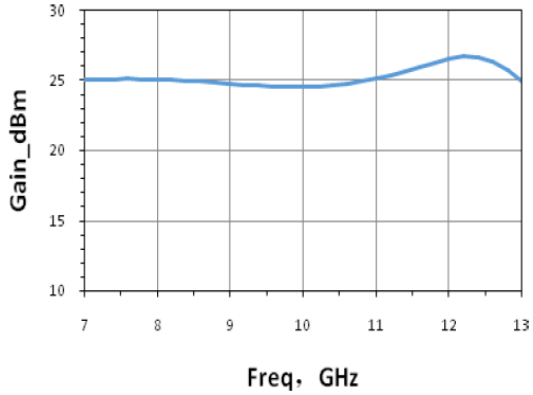
Output Standing Wave Curve



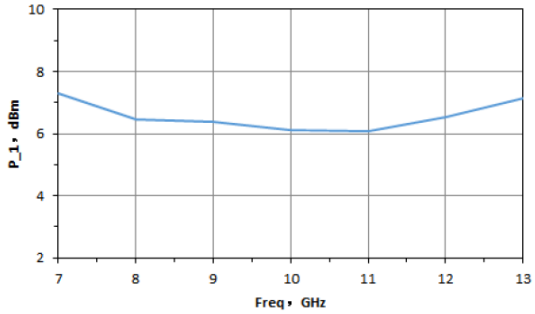
Noise Figure Curve



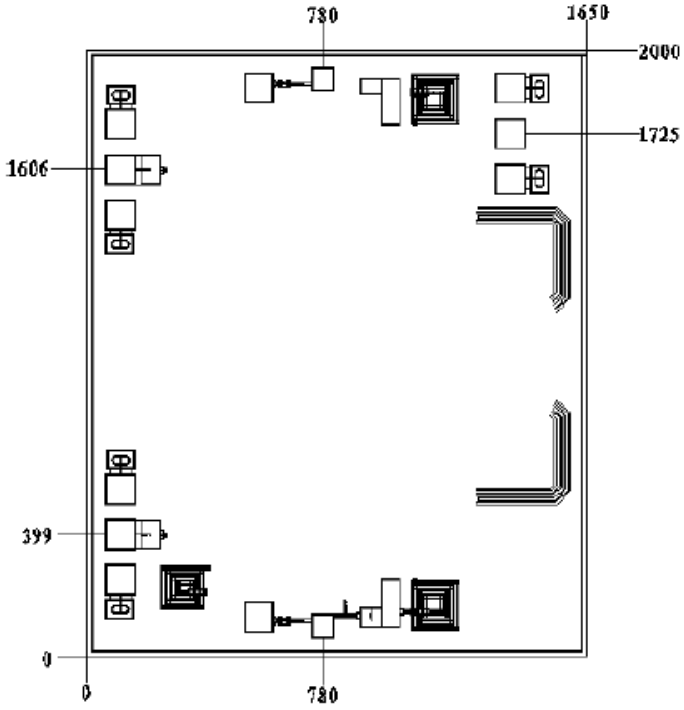
Gain Curve



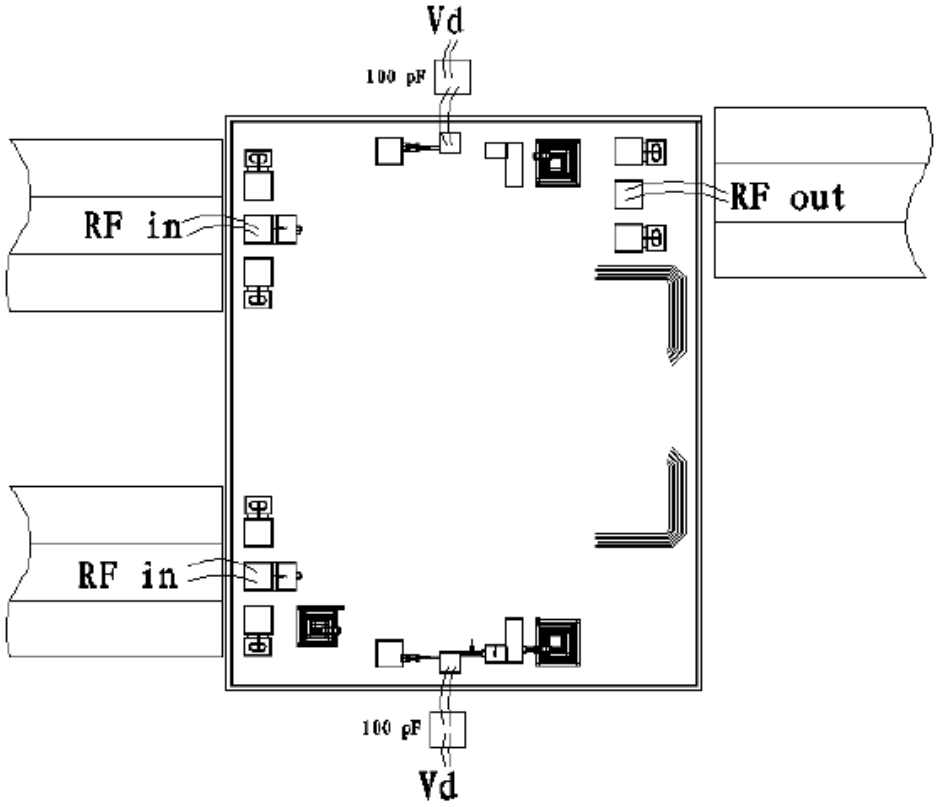
P-1 Compression Characteristic Curve



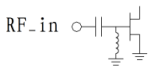
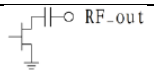
Chip Dimensions (Unit : μm)



Chip Layout Diagram



Pad Definition

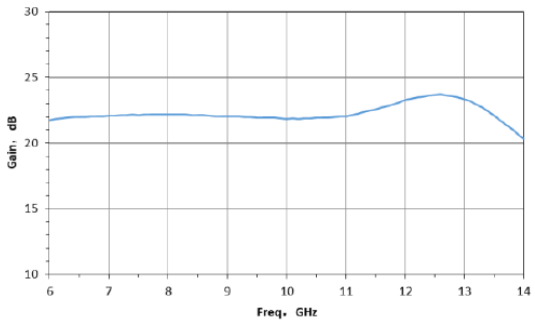
Symbol	Function	Dimension	Equivalent Circuit
RF_in	RF signal input port, connecting to external 50Ω system. no need to add DC blocking capacitor.	100*100μm²	
RF_out	RF signal output port, connecting to external 50Ω system, no need to add DC blocking capacitor.	100*100μm²	
Vd	Amplifier bias, need to connect external 100pF capacitor.	100*100μm²	

[1] See next page for AMLM0008S balance limiter + AMLA0010S balance LNA chipset test.

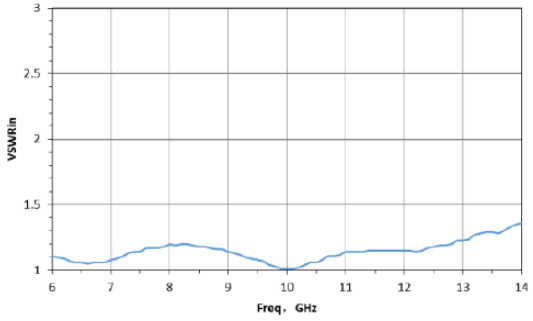
Please see Appendix A for details.

Chipset Typical Test Curve

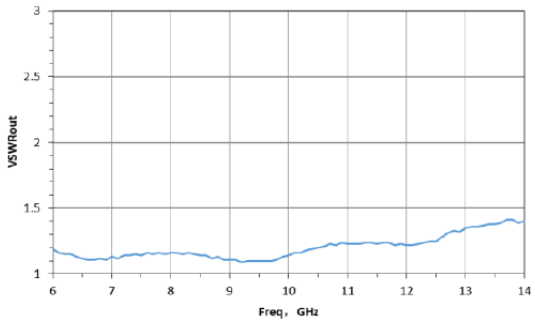
Linear Gain Curve



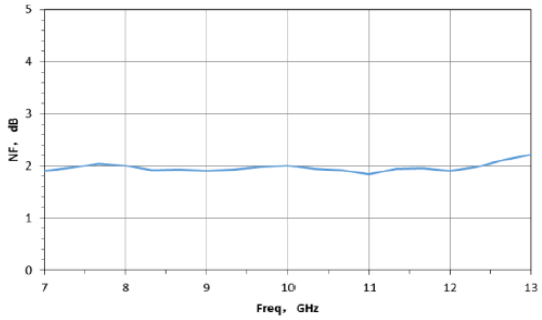
Input Standing Wave Curve



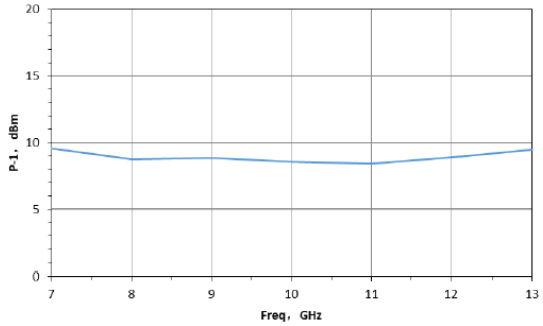
Output Standing Wave Curve



Noise Figure Curve



Output P-1 Curve



Chip Layout Diagram