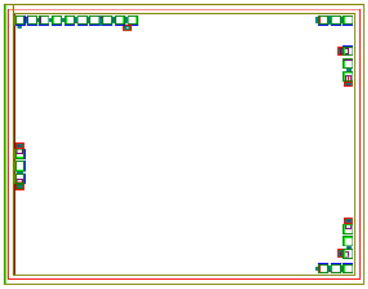
AMT1313

24 - 28GHz Multi-Function Chip



Key Features :

- Frequency range : 24 – 28GHz
- Receiver gain : 12.5dB
- Transmitter gain : 13dB
- Receive/transmit output power at P-1 : 7/9dBm
- Phase shift bit : 6 bits
- Phase shift step : 5.625°
- Phase shift RMS : 3°, phase shift additive attenuation ±1dB
- Attenuation bit : 5 bits
- Attenuation step : 0.5dB
- Attenuation RMS : 0.5dB, attenuation additive phase shift ±5°
- Input/Output Standing Wave : 1.5
- Operating voltage VDD : 5V/30mA
- Operation voltage VSS : -5V/13mA
- Control method : TTL serial control
- Chip dimensions : 4.2mm x 3.2mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1313 is a multi-function chip incorporating with amplifier, switch, 6-digit attenuator, 6-digit phase shifter, control driver etc. functions K band MMIC, it is designed by Gallium Arsenide (GaAs) pHEMT process. The chip uses +5V/-5V voltage operation, control level is TTL, with serial control for phase shift and attenuation, support 40MHz clock signal. This chip is designed with ground through metal vias on the back technology. All chip products p are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
$V_{CLK}/V_{CLR}/V_{SEL}/V_{DARY}/V_{T/R}/V_{DATA}$	Control voltage	+6V	
VDD	Operation voltage	+7V	
VSS	Operation voltage	-6V	
Pin	Max. Input Signal Power	+20dBm	
Tch	Operation Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

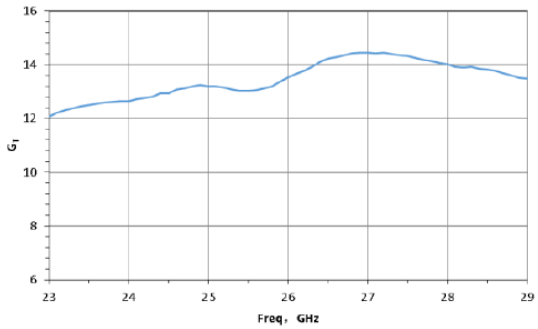
[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

Electrical Characteristics (Ta = 25°C)

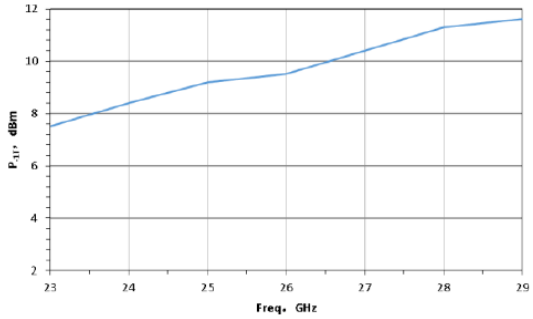
Symbol	Parameter	Value			Unit	Remark
		Min	Typical	Max		
F	Frequency		24 ~ 28		GHz	
G_R	Receiver gain	-	12.5	13	dB	
P_{-1R}	Receiver output at P-1 point	6	7	9	dBm	
NF	Noise figure	-	11	-	dB	
G_T	Transmitter gain	-	13	14.3	dB	
P_{-1T}	Transmitter output at P-1 point	8	9	11	dBm	
PS	Phase shift range	5.625 – 354.375 (6 bits phase shift)			°	
Δat	Phase shift additive attenuation variation	-1	-	+1	dB	
RMS_P	Phase shift RMS	-	3	4.2	°	
ATT	Attenuation range	0.5 – 15.5 (5 bits attenuation)			dB	
Δps	Attenuation additive phase shift variation	-4	-	+4	°	
RMS_A	Attenuation RMS	-	0.2	0.4	dB	
VSWR	Input Output Standing Wave	-	1.5	1.8		
I_D	Operation current Id	-	30	-	mA	Standby state 5mA
I_E	Operation current Is	-	13	-	mA	

Typical Performance

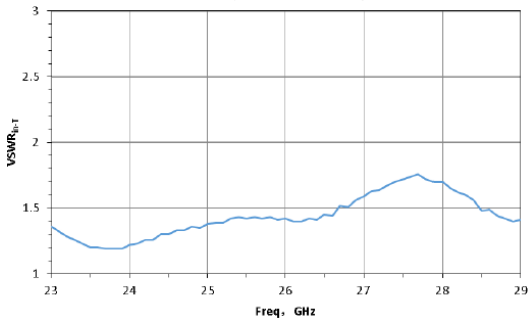
Transmitter Gain Curve



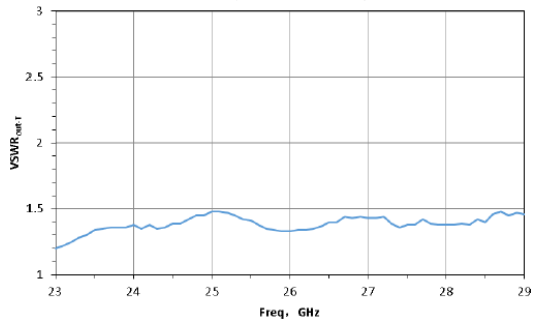
Transmitter P-1 Curve



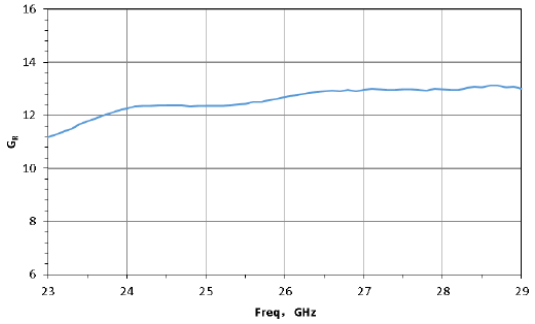
Transmitter Input Standing Wave Curve



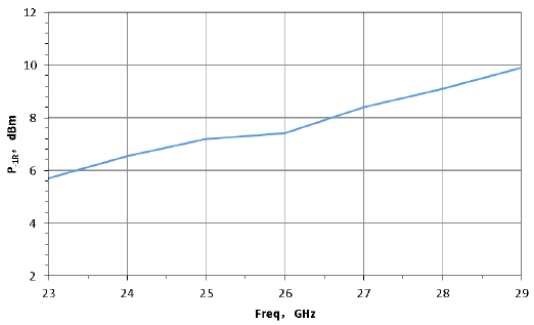
Transmitter Output Standing Wave Curve



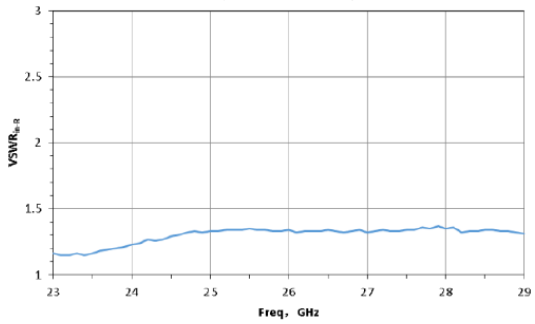
Receiver Gain Curve



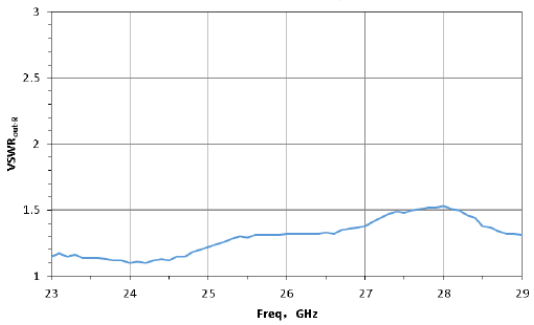
Receiver P-1 Curve



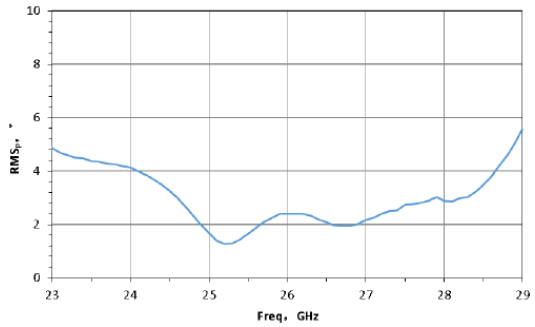
Receiver Input Standing Wave Curve



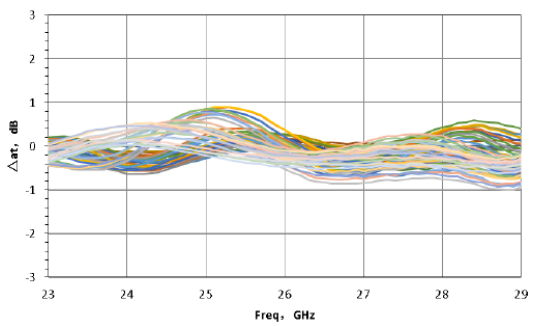
Receiver Output Standing Wave Curve



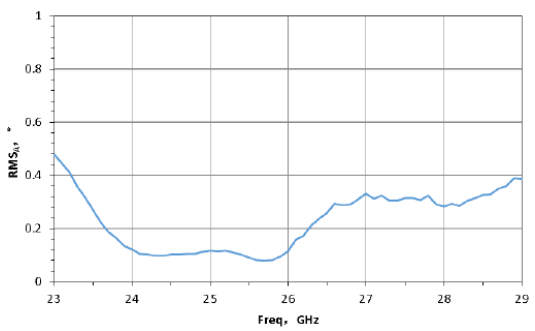
Phase Shift RMS Curve



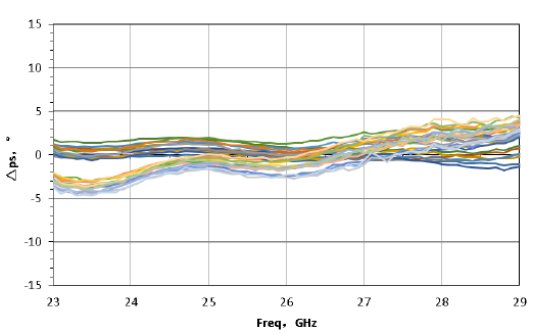
Phase Shift Additive Attenuation Curve



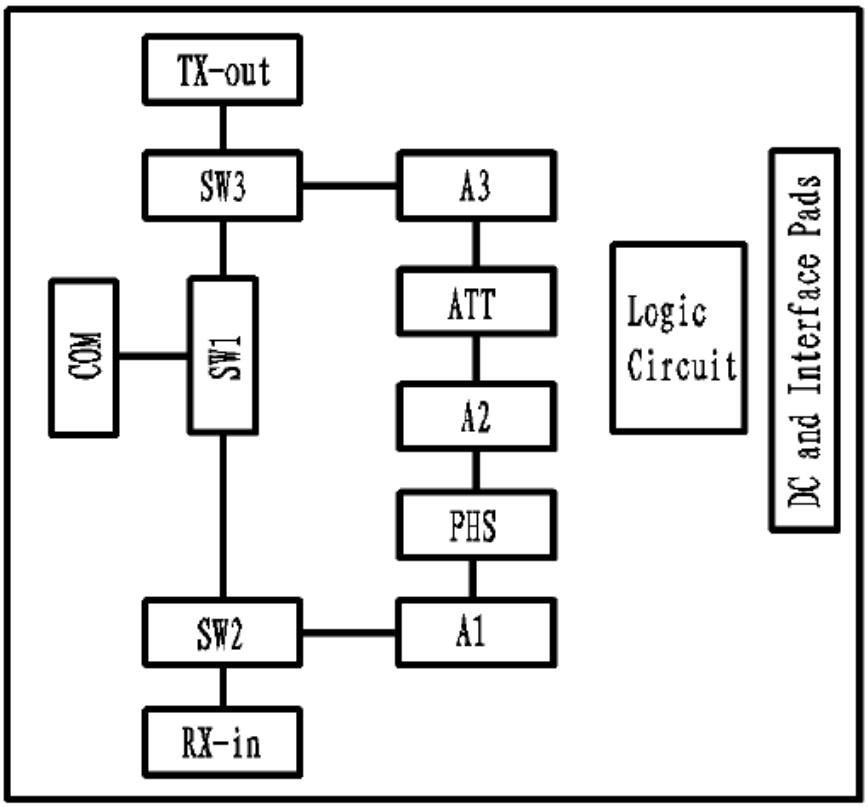
Attenuation RMS Curve



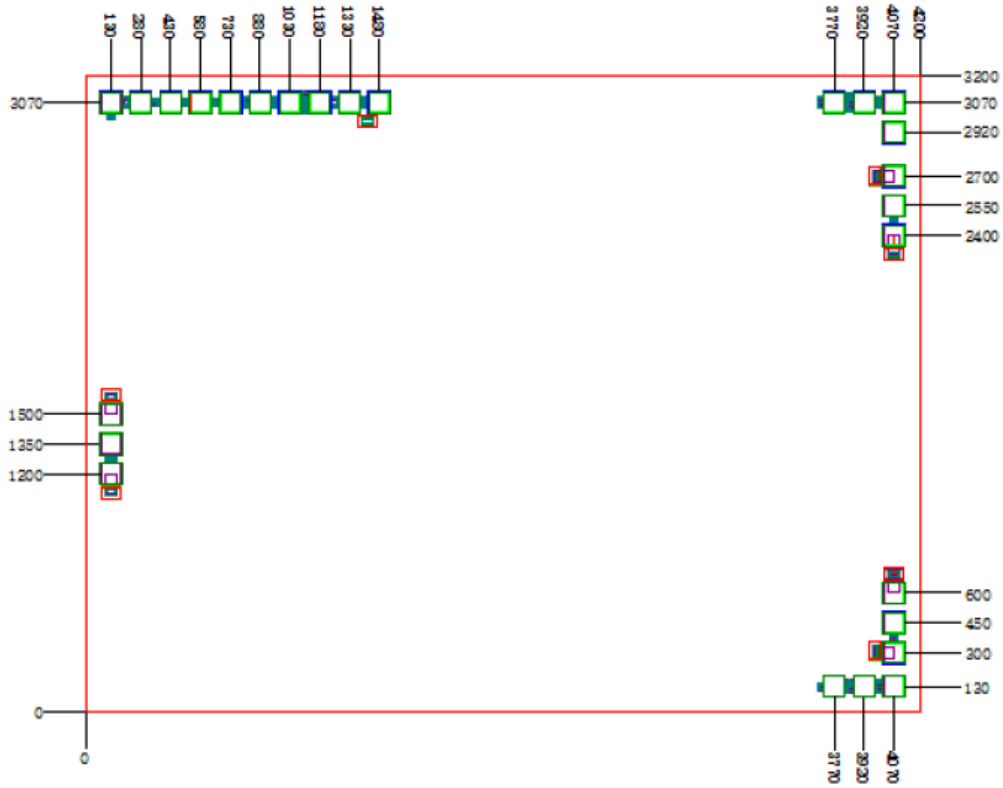
Attenuation Additive Phase Shift Curve



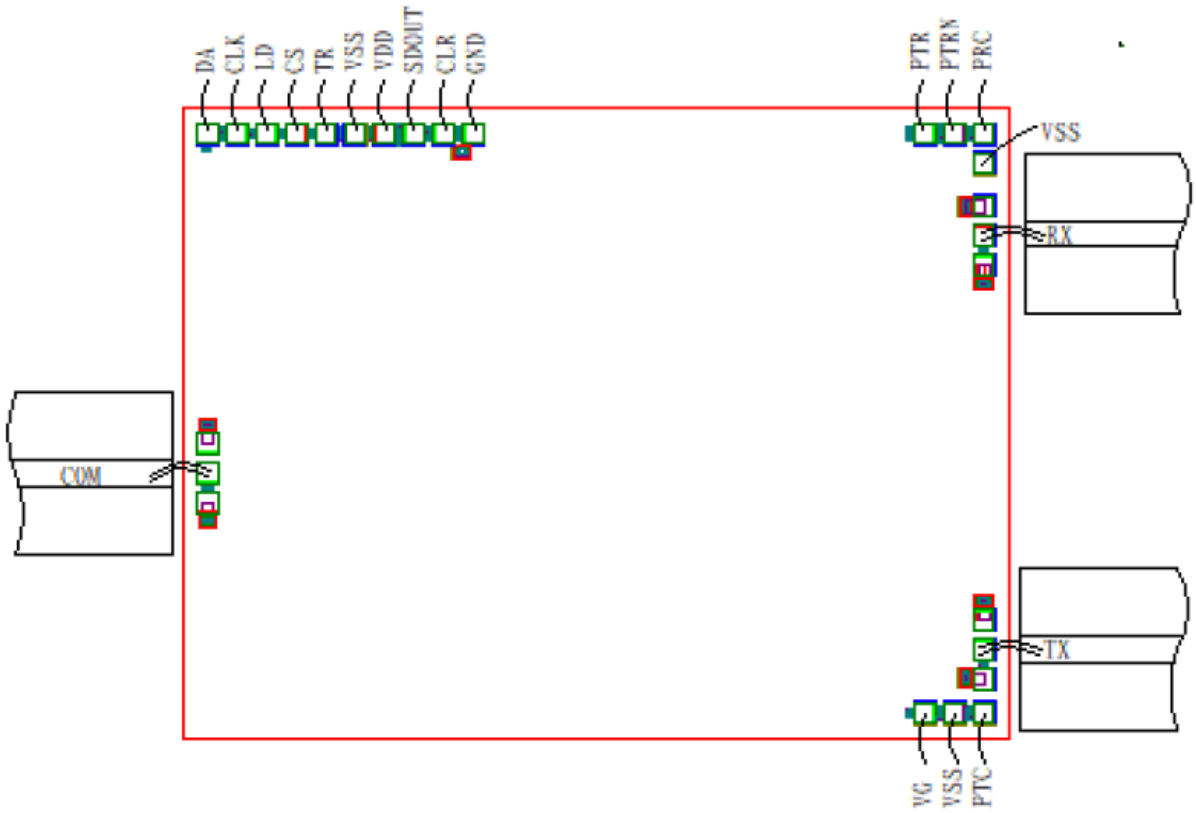
Internal Functional Block Diagram



Chip Dimensions (Unit : µm)



Chip Layout Diagram



Solder Pad Definition

Name	Dimension	Remark
RX_in/TX_out	100μm x 100μm	Receiver Input/Transmitter Output
COM	100μm x 100μm	Receiver Output/Transmitter Input
PTC/PRC/SDOUT	100μm x 100μm	TTL, Output : transmit control/receive control/serial control word
VSS/VDD	100μm x 100μm	Power Supply Pad : -5V/+5V
CS/CLK/DA/LD/TR	100μm x 100μm	TTL, control signal input, speed 40M
CLR	100μm x 100μm	TTL, reset signal input, level high active, can be floating.
GND	100μm x 100μm	Ground
PTR/PTRN	100μm x 100μm	DCFL, TR in-phase/inversion output

Control Description

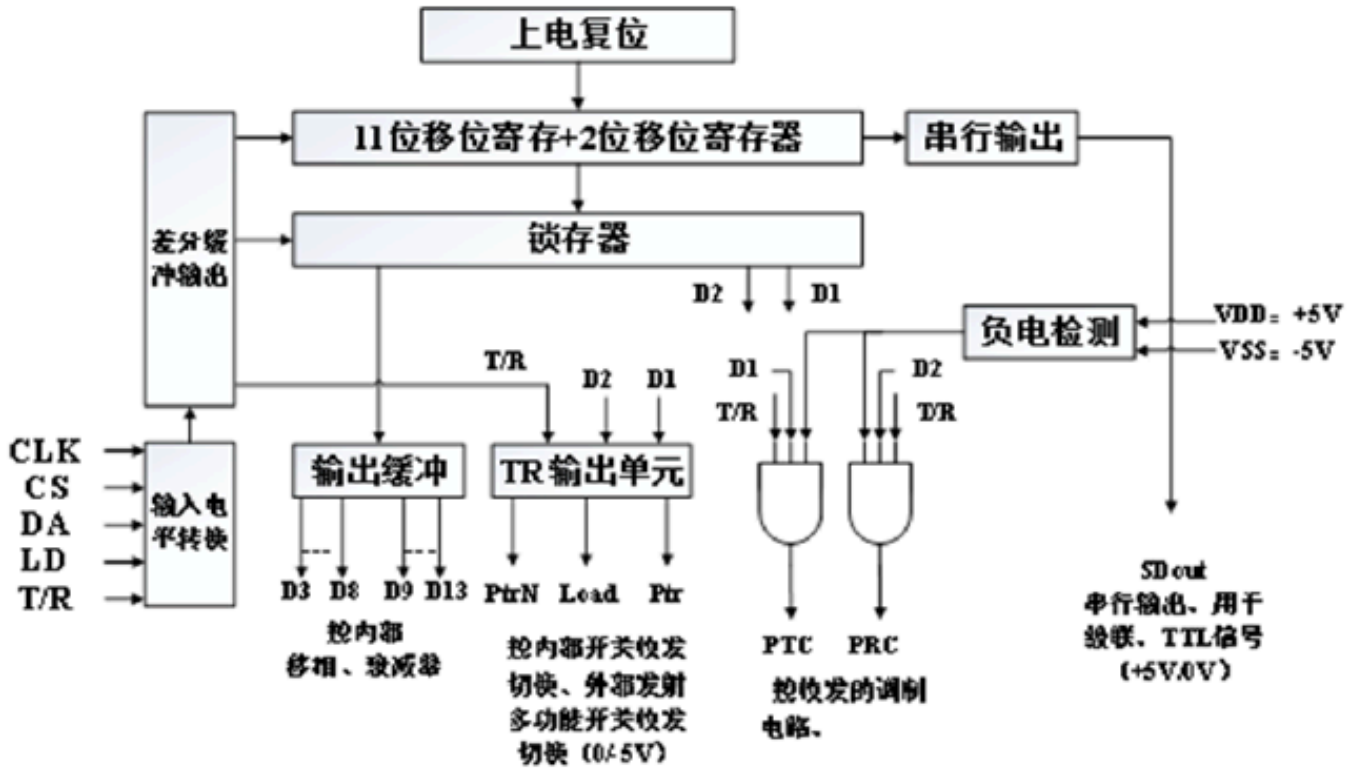
Signal Function Definition

No.	Signal		Level	Function		Remark
				"0"	"1"	
1	TR		Input (TTL Level)	Receive	Transmit	Transmit, receive control signal
2	CS		Input (TTL Level)	Load data	Hold data	Chip select signal, low active
3	CLK		Input (TTL Level)	-		Clock signal, falling edge active
4	LD		Input (TTL Level)	-		Data ready signal, falling edge active
5	DA	Bit 1	Input (TTL Level)	Operate	Standby	Receive enable signal : operate means normal receiving status
		Bit 2 ~ Bit 12	Input (TTL Level)	Off	On	Phase shift attenuation control signal : ON means phase shifter and attenuator enable
		Bit 0	Input (TTL Level)	Operate	Standby	Transmit enable signal : operate means normal transmitting status
6	CLR		Input (TTL Level)	-		Reset signal : 100ms low level after power on, reset activates.
7	PRC		Output (TTL Level)	-		Receive control signal
8	PTC		Output (TTL Level)	-		Transmit control signal
9	SDOUT		Output (TTL Level)	-		Output DA control signal : when new serial control data input into the shift register, the original control data in the register will be output in sequence from SDOUT port.

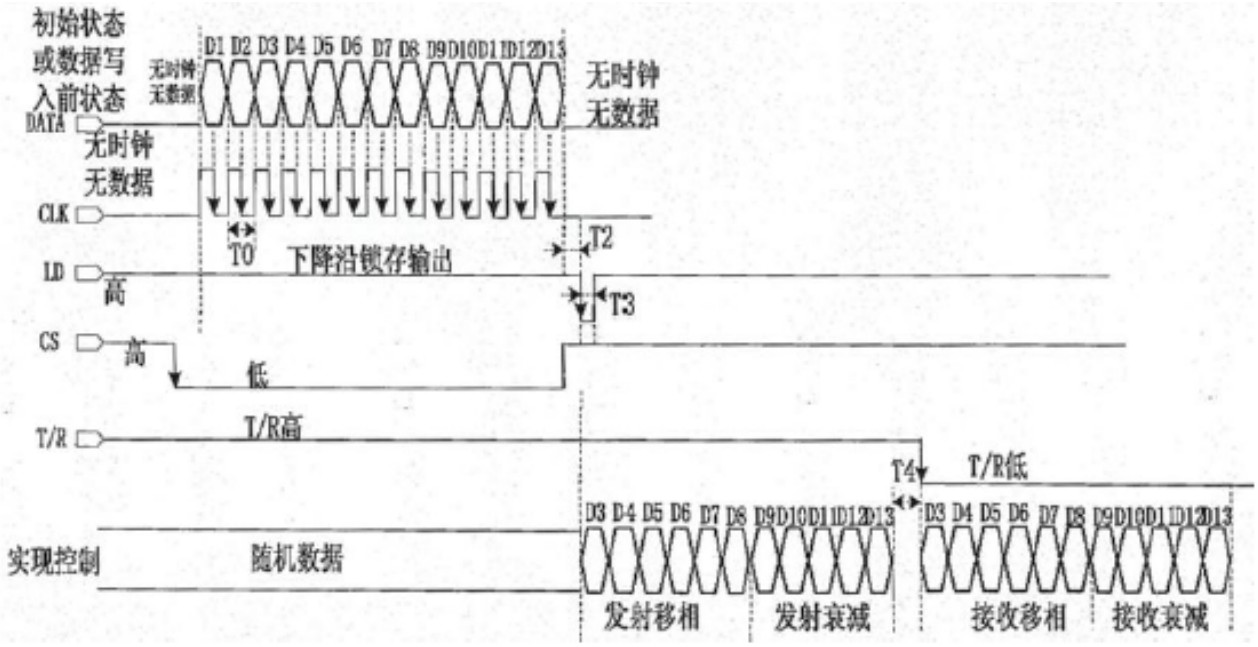
Serial Control Word Definition

BIT	Description	
BIT0	Transmit enable	
BIT1	Receive enable	
BIT2	5.625 °	Phase shift
BIT3	11.25 °	
BIT4	22.5 °	
BIT5	45 °	
BIT6	90 °	
BIT7	180 °	
BIT8	0.5 dB	Attenuation
BIT9	1 dB	
BIT10	2 dB	
BIT11	4 dB	
BIT12	8 dB	

Control Circuit Diagram



Timing



Switch Logic State Truth Table

Input (TTL)			Output			Chip Status
T/R	D1	D2	T/R in-phase output Ptr	T/R inverse output PtrN	LOAD	
1	1	X	0V	-5V	-5V	Transmit state
0	X	1	-5V	0V	-5V	Receive t state
1	0	X	-5V	-5V	0V	Load state
0	X	0	-5V	-5V	0V	Load state

Output Signal Description and State

Input (TTL)			Output (TTL)	
T/R	D1	D2	PTC	PRC
1	1	X	1	0
1	0	X	0	0
0	X	1	0	1
0	X	0	0	0

Please see appendix A for details.