AMT1329
6 – 18GHz Multi-Function Chip

Key Features :

- Frequency range : 6 – 18GHz
- Receiver gain : 7.5dB
- Transmitter gain : 11dB
- Receiver, transmitter P-1 : 9/8dBm
- Phase shift bit : 6 bits
- Phase shift step : 5.625°
- Transmitter phase shift RMS : 5°, transmitter phase shift additive attenuation ±1dB
- Receiver phase shift RMS : 5°, receiver phase shift additive attenuation ±1dB
- Attenuation bit : 6 bits
- Attenuation step : 0.5dB
- Attenuation RMS : 0.8dB, attenuation additive phase shift ±5°
- Input/Output standing wave : 1.5
- Operation voltage VDD/VDN : 5V
- Operation voltage VSN : -5V
- Control method : TTL
- Chip dimensions : 4.8mm x 4.0mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1329 is a multi-function chip incorporating amplifier, switch, 6-digit attenuator, 6-digit phase shifter, control driver etc. functions chip (MMIC), it is designed by Gallium Arsenide (GaAs) pHEMT process. The chip uses +5V/-5V power supply, control level is TTL with serial control for phase shift and attenuation. This chip is designed with ground through metal vias on the back technology. All chip products p are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

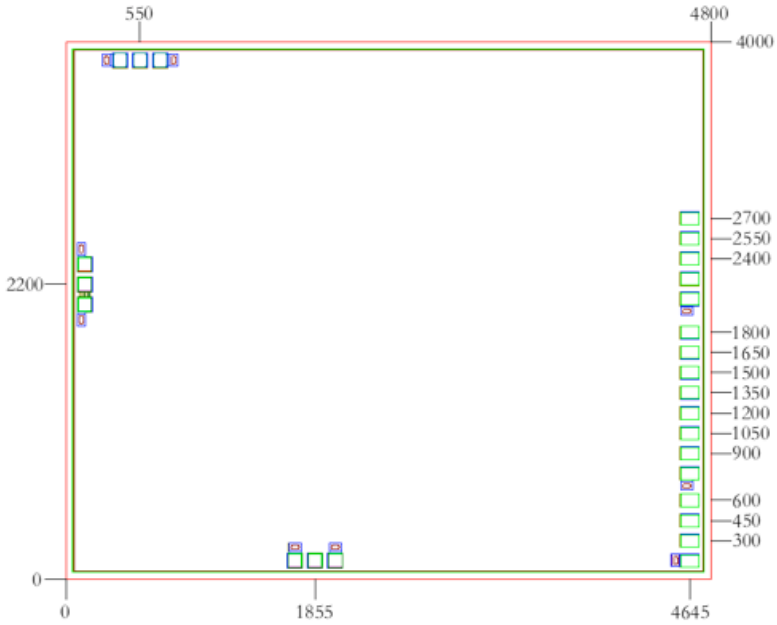
Symbol	Parameter	Value	Remark
$V_{CLK}/V_{CLR}/V_{CS}/V_{LE}/V_{T/R}/V_{DIN}$	Control voltage	+6V	
VDD/VDN	Operating voltage	+7V	
VSN	Operating voltage	-6V	
Pin	Max. Input Signal Power	+20dBm	
Tch	Operating Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

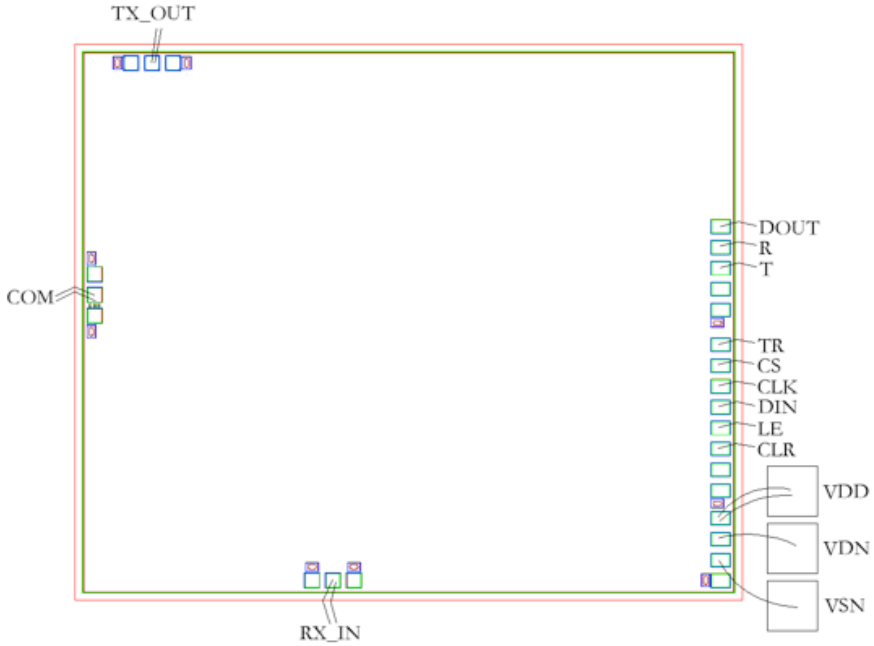
Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Value			Unit	Remark
		Min	Typical	Max		
F	Frequency		6 ~ 18		GHz	
G_R	Receiver gain		7.5		dB	
P_{-1R}	Receiver output at P-1 point		9.5		dBm	
G_T	Transmitter gain		11		dB	
P_{-1T}	Transmitter output at P-1 point		9		dBm	
PS	Phase shift range	5.625 – 354.375 (6 bits phase shift)			°	
ΔatT	Transmitter phase shift additive amplitude variation	-2.5	-	+2.5	dB	
RMS_{PT}	Transmitter phase shift RMS	-	5	-	°	
ΔatR	Receiver phase shift additive amplitude variation	-2.5	-	+2.5	dB	
RMS_{PR}	Phase shift RMS	-	5	-	°	
ATT	Attenuation range	0.5 – 31.5 (6 bits attenuation)			dB	
Δps	Attenuation additive phase shift varation	-10	-	+10		
RMS_A	Attenuation RMS	-	0.8	-	dB	
VSWR	Input/Output standing wave	-	1.5	-	-	
Id	Drain current	-	55	-	mA	

Chip Dimensions (Unit : µm)



Chip Layout Diagram



Pad Definition

Name	Dimension	Description
RX_in/TX_out	100µm x 100µm	Receiver input/ Transmitter output
COM	100µm x 100µm	Receiver output/ Transmitter input
R/T/DOUT	100µm x 140µm	TTL, separate output : Receive Standby/Transmit Standby/Serial Control word
VSN/VDN/VDD	100µm x 140µm	Supply pad : -5V/+5V/+5V
CS/CLK/DIN/LE/TR	100µm x 140µm	TTL, control signal input, speed 40M
CLR	100µm x 140µm	TTL, reset signal input

Control Descriptions

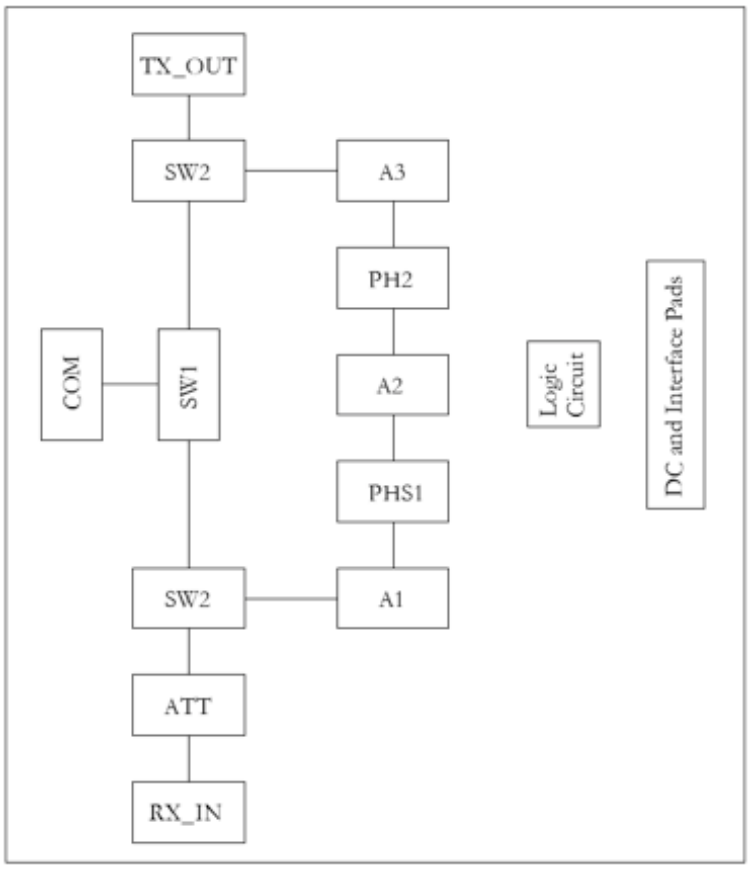
Signal Function Definition

No.	Singal		Level	Function		Remark
				"0"	"1"	
1	TR		Input (TTL level)	Receive	Transmit	Transmit, receive control signal
2	CS		Input (TTL level)	Add data	Keep data	Chip select signal, low active
3	CLK		Input (TTL level)	-		Clock signal, falling edge active
4	LE		Input (TTL level)	-		Data ready signal, rise edge active
5	DIN	Bit 18	Input (TTL level)	-	Operate	Receive enable signal : operate means normal receive status
		Bit 0 ~ Bit 17	Input (TTL level)	Off	On	Phase shift attenuation control signal : ON means Shifter and Attenuator operate.
		Bit 19	Input (TTL level)	-	Operate	Transmit enable signal : operate means normal transmit status
6	CLR		Input (TTL level)	-		Reset signal : power up 100ms low level, reset starts.
7	R		Output (TTL level)	-		Receive control signal
8	T		Output (TTL level)	-		Transmit control signal
9	DOUT		Output (TTL level)	-		Output DIN control signal : when new serial control word is sent into phase shift register, original control word stored in the register will output from DOUT port.

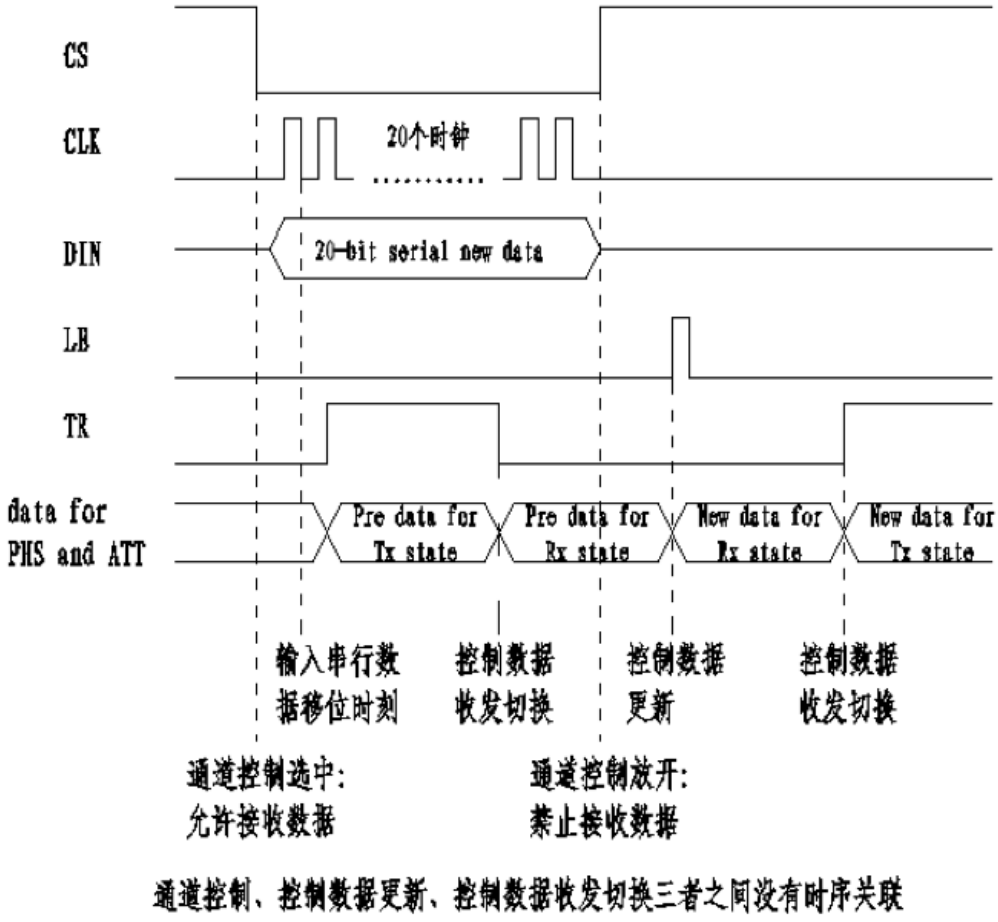
Serial Data Definition

BIT	Description	
BIT0	5.625°	Transmit phase shift
BIT1	11.25°	
BIT2	22.5°	
BIT3	45°	
BIT4	90°	
BIT5	180°	
BIT6	5.625°	Receive phase shift
BIT7	11.25°	
BIT8	22.5°	
BIT9	45°	
BIT10	90°	
BIT11	180°	
BIT12	0.5dB	Receive attenuation
BIT13	1dB	
BIT14	2dB	
BIT15	4dB	
BIT16	8dB	
BIT17	16dB	
BIT18	Receiver standby	R output
BIT19	Transmit standby	T output

Internal Block Diagram



Timing Diagram



Please see Appendix A for details.