AMT1A01

5 ~ 6GHz Balanced Type Limited Amplitude LNA Chip

Key Features :

- Frequency range : 5～6GHz
- Typical gain : 27dB
- Input standing wave : 1.2
- Output standing wave : 1.3
- Noise figure : 1.1dB
- Output at P-1 : 10.5dBm @ +5V/24mA
- Endurance power : 25W (CW)
- Chip dimensions：2.4mm*1.0mm*0.1mm
- Application : microwave transceiver, wireless communication etc.

Description :

AMT1A01 is a GaAs high performance balanced type limited amplitude low noise amplifier chip, with operating frequency in 5~6GHz, 1.1dB noise figure, 27dB typical gain, it integrates limitor and LNA, supply can be applied to both sides. It is designed with ground through metal via on the back technology.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	+7V	
Pin	Input Signal Power	42dBm	
Tch	Operating Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage

Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Test Condition	Value			Unit
			Min	Typical	Max	
Gain	Small signal gain	VDD = +5V F : 5 ~ 6GHz	-	27	-	dB
NF	Noise figure		-	1.1	-	dB
Id	Operating current		-	24	-	mA
VSWRin	Input standing wave		-	1.2	-	-
VSWRout	Output standing wave		-	1.3	-	-
P-1	1dB compression output			10.5	-	dBm

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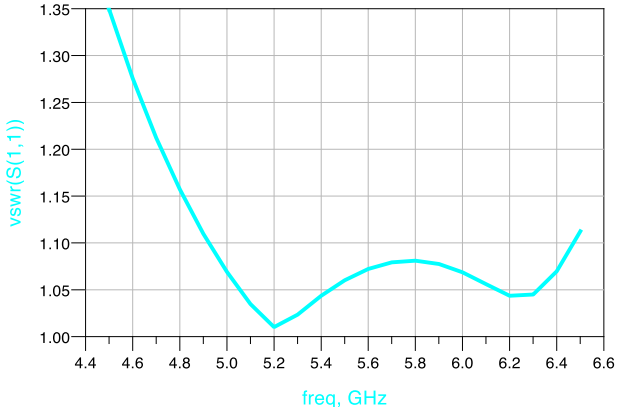
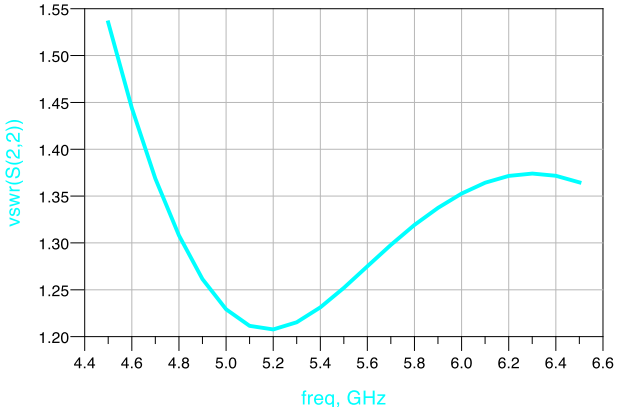
Typical Performance

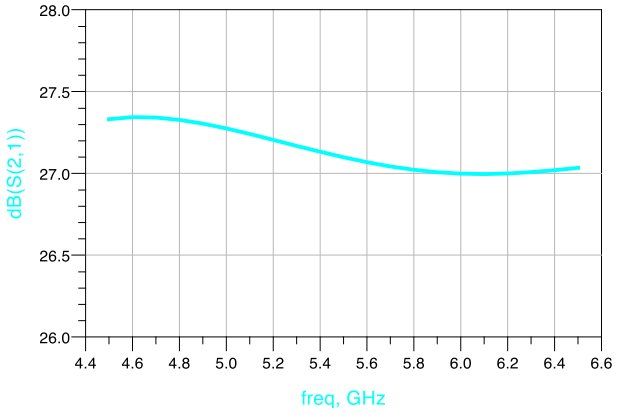
Input Standing Wave Curve



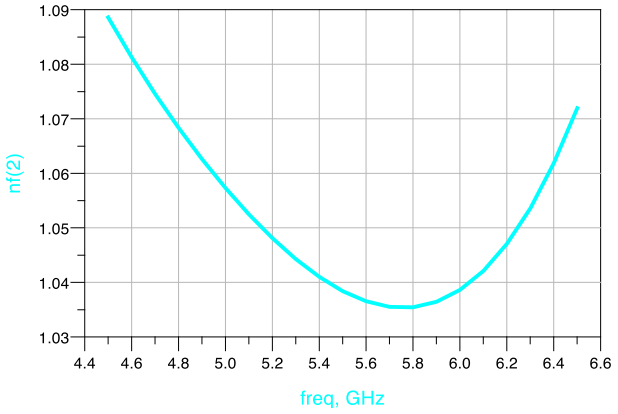
Output Standing Wave Curve



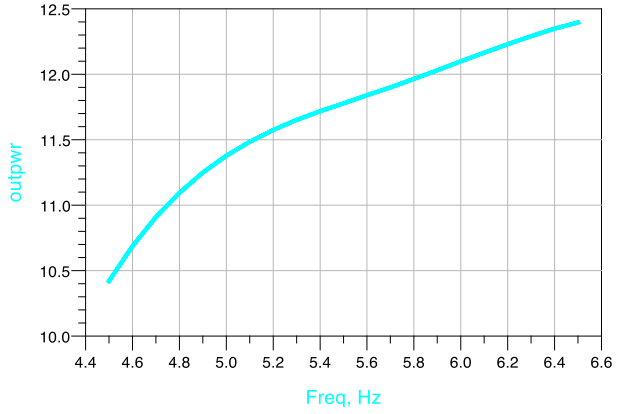
Linear Gain Curve



Noise Figure Curve



P-1 Output Curve



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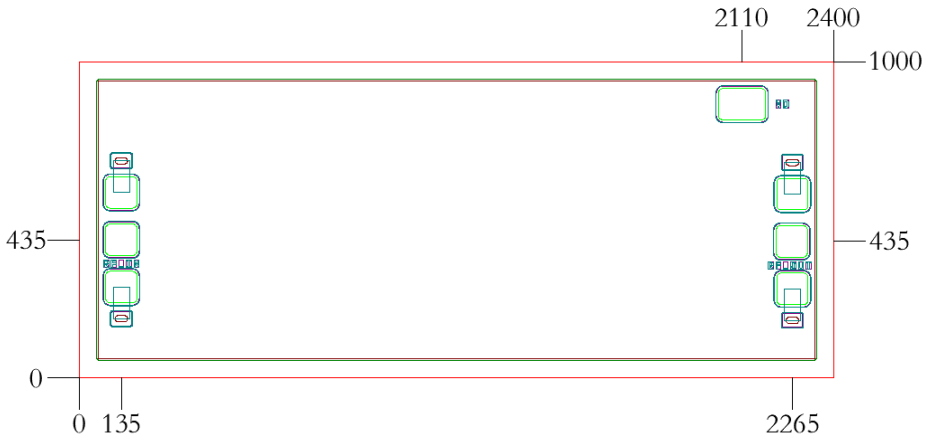
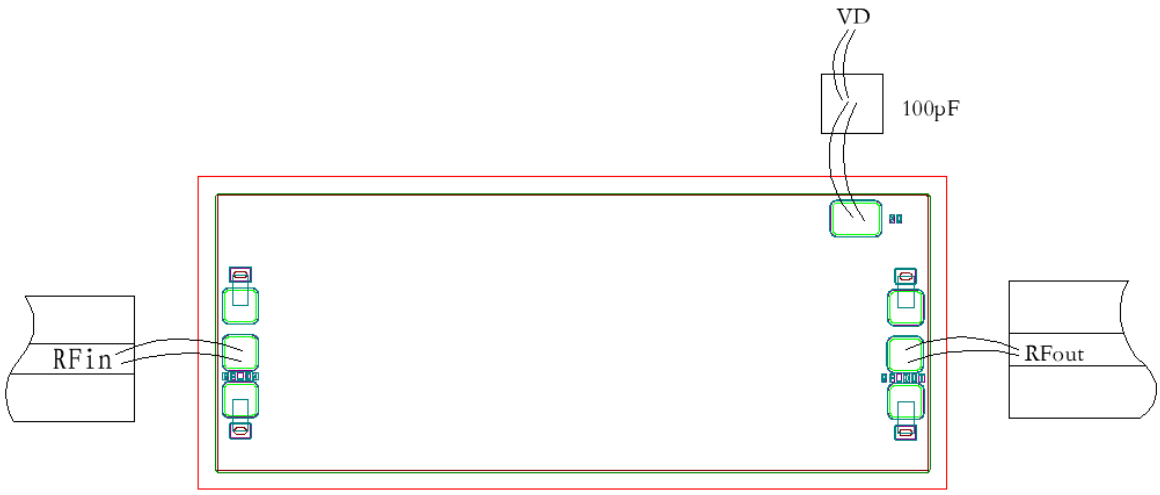
Chip Dimension (Unit : μm)



Chip Layout Diagram



Pad Definition

Pad No.	Symbol	Function	Dimension
1	RFin	RF signal input port, connecting to external 50Ω system, internal built-in DC blocking capacitor.	100*100μm^2
2	RFout	RF signal output port, connecting to external 50Ω system, internal build-in DC blocking capacitor.	100*100μm^2
3	VD	+5V amplifier bias, need to connect to external 100pF capacitor.	100*100μm^2

Please see Appendix A for details.