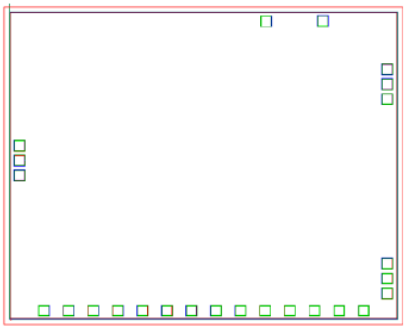
AMT1312

14 - 18GHz Multi-Function Chip



Key Features :

- Frequency range : 14 – 18GHz
- Receiver gain : 5dB
- Transmitter power gain : 32dB
- Receiver at P-1 : 5dBm
- Transmitter channel saturated output power Psat : 33dBm
- Phase shift bit : 6 bits
- Phase shift step : 5.625°
- Phase shift RMS : 3.5°, phase shift additive attenuation ±2dB
- Attenuation bit : 6 bits (for receive only)
- Attenuation step : 0.5dB (for receive only)
- Attenuation RMS : 0.7dB, attenuation additive phase shift ±10° (for receive only)
- Input/output standing wave : 1.6
- Operating voltage VDD/VDN: 5V
- Operation voltage VSN : -5V
- Control method : TTL
- Chip dimensions : 4.05mm x 3.2mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1312 is a multi-function chip incorporating with amplifier, switch, 6-digit attenuator, 6-digit phase shifter, control driver etc. functions Ku band MMIC, it is designed by Gallium Arsenide (GaAs) pHEMT process. The chip uses +5V/-5V voltage operation, control level is TTL, with serial control for phase shift and attenuation. This chip is designed with ground through metal vias on the back technology. All chip products p are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

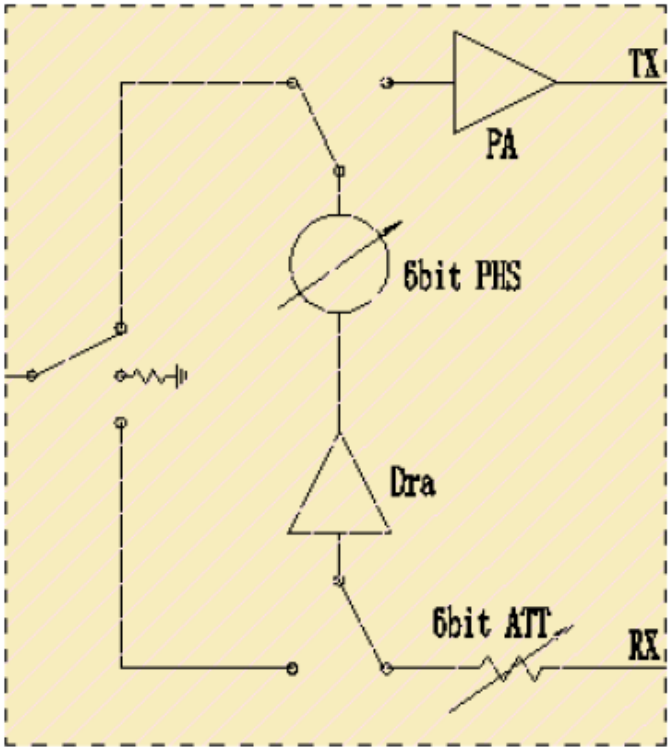
Symbol	Parameter	Value	Remark
$V_{CLK}/V_{CLR}/V_{CS}/V_{LE}/V_{T/R}/V_{DIN}$	Control voltage	+6V	
VDD	Operation voltage	+7V	
VSN	Operation voltage	-6V	
Pin	Max. Input Signal Power	+20dBm	
Tch	Operation Temperature	150℃	
Tm	Sintering Temperature	310℃	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150℃	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

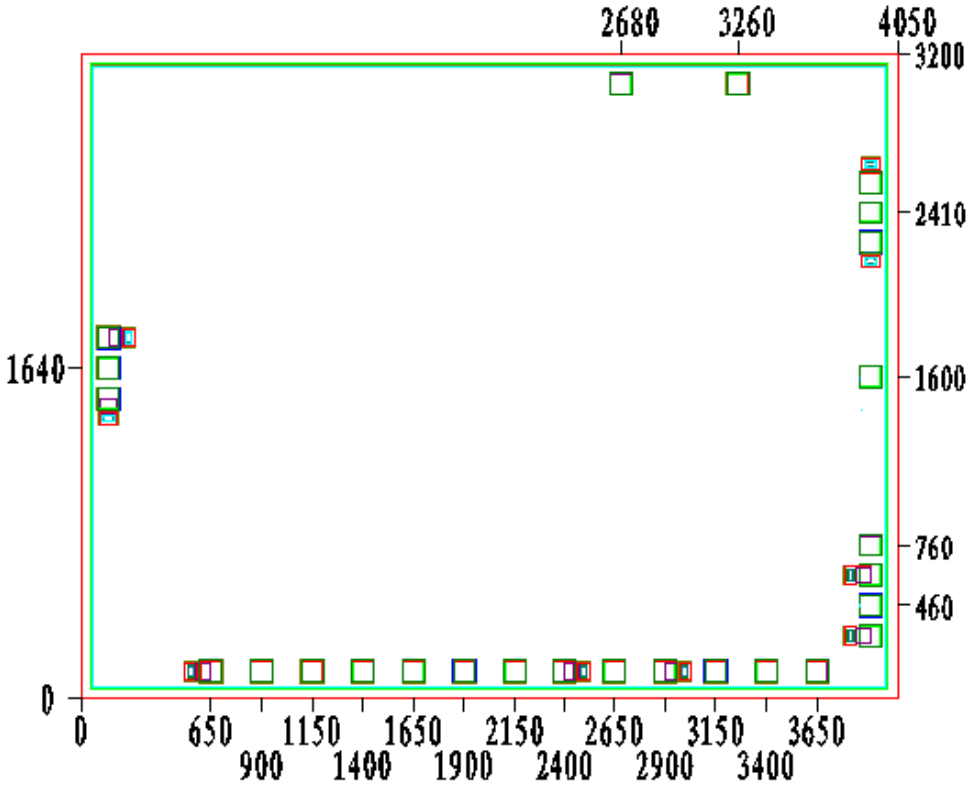
Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Value			Unit	Remark
		Min	Typical	Max		
F	Frequency		14 ~ 18		GHz	
G_R	Receiver gain	-	5	-	dB	
P_{-1R}	Receiver output at P-1 point	-	5	-	dBm	
NF	Noise figure	-	9	-	dB	
G_T	Transmitter gain	-	32	-	dB	
P_{-1T}	Transmitter output at P-1 point	-	33	-	dBm	
PS	Phase shift range	5.625 – 354.375 (6 bits phase shift)			°	
Δat	Phase shift additive attenuation variation	-2.5	-	+2.5	dB	
RMS_P	Phase shift RMS	-	3.5	-	°	
ATT	Attenuation range	0.5 – 31.5 (6 bits attenuation)			dB	
Δps	Attenuation additive phase shift variation	-10	-	+10	°	
RMS_A	Attenuation RMS	-	0.7	-	dB	
VSWR	Input Output Standing Wave	-	1.6	-		
I_d	Operation current Id	-	30	-	mA	
I_s	Operation current Is	-	18	-	mA	
I_{dn}	Operation current Idn	-	870	-	mA	

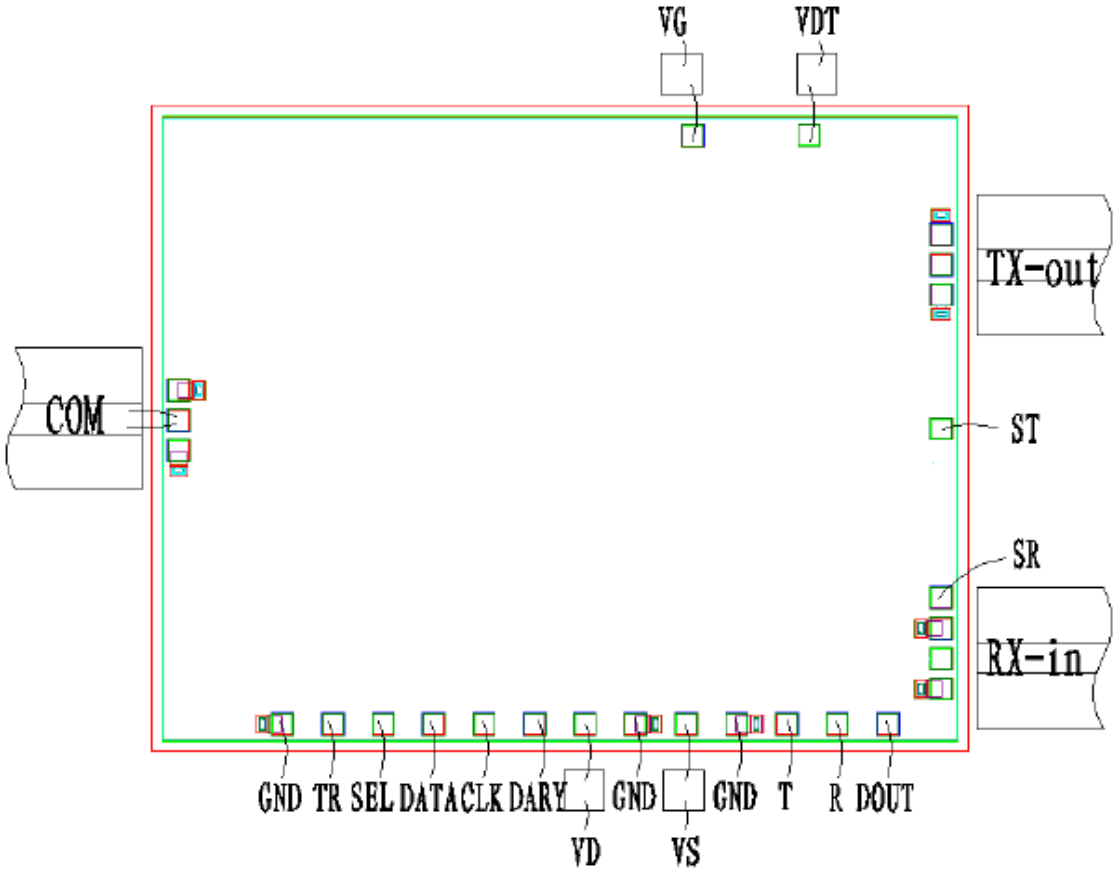
Internal Functional Block Diagram



Chip Dimensions (Unit : μm)



Chip Layout Diagram



Control Description

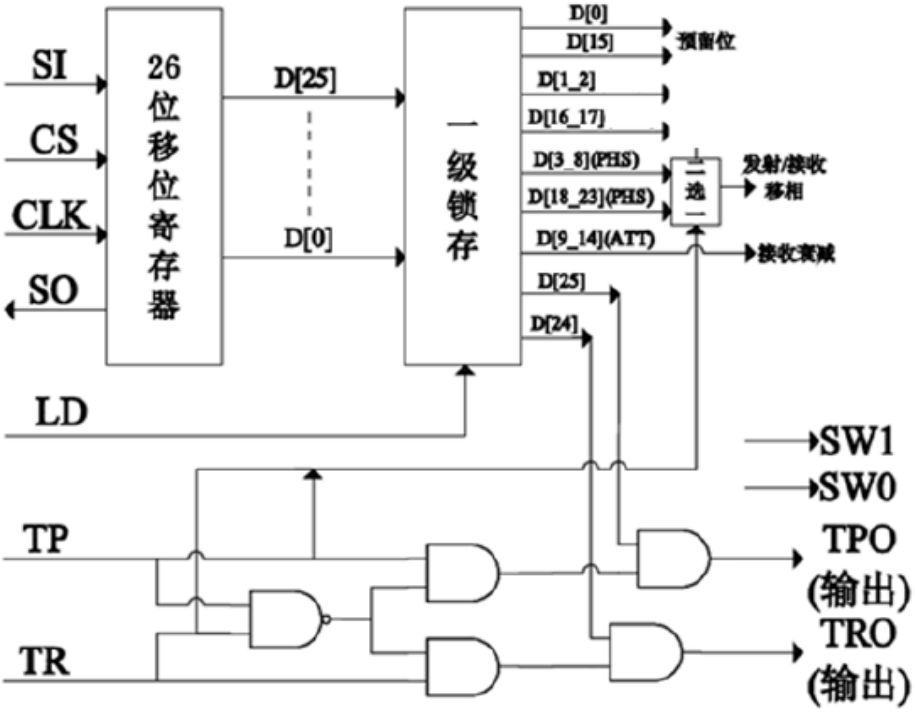
Signal Function Definition

No.	Signal		Level	Function		Remark
				"0"	"1"	
1	TR		Input (TTL Level)	Receive	Transmit	Transmit, receive control signal
2	SEL		Input (TTL Level)	Load data	Hold data	Chip select signal, low active
3	CLK		Input (TTL Level)	-		Clock signal, falling edge active
4	DARY		Input (TTL Level)	-		Data ready signal, rising edge active
5	DATA	Bit 18	Input (TTL Level)	-	Operate	Receive enable signal : Operate means normal receiving status
		Bit 0 ~ Bit 17	Input (TTL Level)	Off	On	Phase shift attenuation control signal : ON means phase shifter and attenuator enable
			Input (TTL Level)			
		Bit 19	Input (TTL Level)	-	Operate	Transmit enable signal : operate means normal transmitting status
6	CLR		Input (TTL Level)	-		Reset signal : 100ms low level after power on, reset activates.
7	R		Output (TTL Level)	-		Receive control signal
8	T		Output (TTL Level)	-		Transmit control signal
9	DOUT		Output (TTL Level)	-		Output DIN control signal : when new seria control data input into the shift register, the original control data in the register will be output in sequence from DOUT port.
10	ST		Output (0/-5V)	-		Transmit switch control signal
11	SR		Output (0/-5V)	-		Receive switch control signal

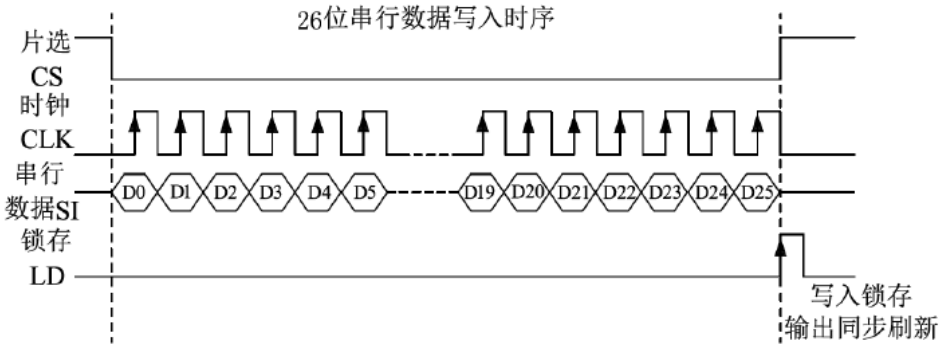
Serial Control Word Definition

BIT	Description	
BIT0	-	Reserved bit
BIT1	25ps	Receive delay
BIT2	50ps	
BIT3	5.625 °	Receive phase shift
BIT4	11.25 °	
BIT5	22.5 °	
BIT6	45 °	
BIT7	90 °	
BIT8	180 °	
BIT9	0.5 dB	Receive attenuation
BIT10	1 dB	
BIT11	2 dB	
BIT12	4 dB	
BIT13	8 dB	
BIT14	16 dB	
BIT15	-	Reserved bit
BIT16	25ps	Transmit delay
BIT17	50ps	
BIT18	5.625 °	Transmit phase shift
BIT19	11.25 °	
BIT20	22.5 °	
BIT21	45 °	
BIT22	90 °	
BIT23	180 °	
BIT24	RXEN	Receive enable
BIT25	TXEN	Transmit enable

Control Circuit Diagram



Timing



说明：

●时钟CLK上升沿移位数据,LD上升沿刷新数据；

●CS为片选信号，低电平有效。当CS状态发生变化时，CLK信号为低电平，以避免在内部时钟上带来毛刺，导致数据移位异常。

Please see appendix A for details.