AMT1328
33-37GHz Transceiver Integrated Multi-Function Chip


## Key Features :

- Frequency : 33-37GHz
- Receiver gain : 25 dB
- Transmitter gain : 28dB
- Receiver noise figure : 3.8 dB
- Receiver input/output standing wave :1.5/1.5
- Transmitter input/output standing wave : 1.4/1.4
- Receiver output power at P-1:13dBm
- Transmitter output power at P-1:19dBm
- Transmitter saturated output power: 21.5 dBm
- Receiver power dissipation : $5 \mathrm{~V} / 90 \mathrm{~mA}$
- Transmitter power dissipation : 5V/120mA
- Switch control method: 0/-5V
- Chip dimensions : $3.0 \mathrm{~mm} \times 2.5 \mathrm{~mm} \times 0.1 \mathrm{~mm}$
- Applications : wireless communication, transceiver module, radio telecommunication etc.


## Description :

AMT1328 is a high performance transceiver multi-function chip, frequency range is $33-37 \mathrm{GHz}$, it integrates switch and bi-directional power amplifier, receiver gain is 25 dB , noise figure is 3.8 dB , transmitter gain is 28 dB , and transmitter saturated output power is 21.5 dBm . It is designed by Gallium Arsenide (GaAs) process. This chip is designed with ground through metal vias on the back technology. All chip products $p$ are $100 \%$ RF tested.

Absolute Maximum Ratings ( $\mathbf{T a}=25^{\circ} \mathrm{C}$ )

| Symbol | Parameter | Value | Remark |
| :---: | :---: | :---: | :---: |
| Vd | Drain voltage | +7 V |  |
| Pin | Max. Input Signal Power | 12 dBm |  |
| Tch | Operation Temperature | $150^{\circ} \mathrm{C}$ |  |
| Tm | Sintering Temperature | $310^{\circ} \mathrm{C}$ | $30 \mathrm{~s}, \mathrm{~N}_{2}$ protection |
| Tstg | Storage Temperature | $-65^{\sim}+150^{\circ} \mathrm{C}$ |  |

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

Electrical Characteristics $\left(\mathbf{T a}=25^{\circ} \mathrm{C}\right)$

| Symbol | Parameter | Test Conditions | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typical | Max |  |
| $\mathrm{G}_{\mathrm{R}}$ | Receiver gain | $\begin{aligned} & \text { F: } 6 \sim 18 G H z \\ & \text { PA_VD1 }=0 \mathrm{~V}, \text { PA_VD2 }= \\ & \text { OV, PA_VD3 }=0 \mathrm{~V}, \\ & \text { PA_VD4 }=0 \mathrm{~V}, \mathrm{PA} \text {,VG = } \\ & \text { OV, LNA_VD }=+5 \mathrm{~V}, \mathrm{SW} 1 \\ & =0 \mathrm{~V}, \mathrm{SW} 2=-5 \mathrm{~V} \\ & \hline \end{aligned}$ | - | 26 | - | dB |
| NF | Receiver noise figure |  | - | 3.5 | - | dB |
| VSWR ${ }_{\text {Rx }}$ | Receiver input standing wave |  | - | 1.4 | - | - |
| VSWR ${ }_{\text {RX }}$ | Receiver output standing wave |  | - | 1.4 | - | - |
| $\mathrm{P}_{\mathrm{R}-\mathrm{ddB}}$ | Receiver output power at P-1 point |  | - | 2.5 | - | dBm |
| $\mathrm{G}_{\mathrm{T}}$ | Transmitter power gain | $\begin{aligned} & \mathrm{F}: 6^{\sim} 18 \mathrm{GHz}, \mathrm{PA} \text { VD1 }= \\ & +5 \mathrm{~V}, \mathrm{PA} \text { VDD }=+5 \mathrm{~V}, \\ & \text { PA_VD3 }=+5 \mathrm{~V}, \text { PA_VD4 } \\ & =+5 \mathrm{~V}, \mathrm{PA} \text { _VG }=-5 \mathrm{~V}, \\ & \text { LNA_VD }=0 \mathrm{~V}, \text { SW1 }=- \\ & 5 \mathrm{~V}, \mathrm{SW} 2=0 \mathrm{~V} \end{aligned}$ | - | 23 | - | dB |
| VSWR ${ }_{\text {TX }}$ | Transmitter input standing wave |  | - | 1.8 | - | - |
| $\mathrm{VSWR}_{\text {TX }}$ | Transmitter output standing wave |  | - | 2 | - | - |
| $\mathrm{P}_{\mathrm{T}-1 \mathrm{~dB}}$ | Transmitter output power at P-1 point |  | - | 22 | - | dBm |
| Pout | Transmitter saturated output power |  | - | 0.5 | - | A |

## Typical Performance



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Chip Dimensions (Unit : $\mu \mathrm{m}$ )


## Chip Layout Diagram



## Pad Definition

| Symbol | Function Description | Dimensions |
| :---: | :---: | :---: |
| RF1 | RF signal transmitter input/receiver output port, external connecting to $50 \Omega$ system. | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| RR2 | RF signal receiver input/transmitter output port, external connecting to $50 \Omega$ system. | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| PA_VD1 | Amplifier voltage bias at transmit state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| PA_VD2 | Amplifier voltage bias at transmit state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| PA_VD3 | Amplifier voltage bias at transmit state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| PA_VD4 | Amplifier voltage bias at transmit state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| PA_VG | Amplifier voltage bias at transmit state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| LNA_VD | Amplifier voltage bias at receive state, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| SW1 | Supply control port, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |
| SW2 | Supply control port, refer to usage explanation for control logic | $100 \mu \mathrm{~m} * 100 \mu \mathrm{~m}$ |

## Usage Explanation

| Operation State | Receive State (RF2-RF1) | Transmit State (RF1-RF2) |
| :---: | :---: | :---: |
| Voltage bias | PA_VD1 = 0V, PA_VD2 = 0V, PA_VD3 = 0V, PA_VD4 $=0 \mathrm{~V}, \mathrm{PA} \_\mathrm{VG}=0 \mathrm{~V}, \mathrm{LNA}$ VD $=+5 \mathrm{~V}$, SW1 $=0 \mathrm{~V}, \mathrm{SW} 2=-5 \mathrm{~V}$ | PA_VD1 $=+5 \mathrm{~V}, \mathrm{PA}$ VD2 $=+5 \mathrm{~V}, \mathrm{PA} \_\mathrm{VD} 3=+5 \mathrm{~V}$ PA_VD4 $=+5 \mathrm{~V}, \mathrm{PA} \_\mathrm{VG}=-5 \mathrm{~V}, \mathrm{LNA}$ VD $=0 \mathrm{~V}$, SW1 $=-5 \mathrm{~V}, \mathrm{SW} 2=0 \mathrm{~V}$ |

Note, use either one of SW1 / SW2.
Please see appendix A for details.

[^1]
[^0]:    Advanced Microsystems Technology reserves the right to make change of data and information in the datasheet without prior notice.
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