AMT2105 7 – 12GHz Power Amplifier Chip



Key Features:

Frequency: 7 – 12GHz

Typical small signal gain: 33dBTypical output power: 47.5dBm

• Typical power added efficiency: 42%@7-10GHz

37%@10-12GHz

Supply voltage: 28V, -2.2V

• Chip dimensions: 4.1mm x 4.7mm x 0.1mm

• Applications: wireless communication, transceiver module, radio telecommunication etc.

Description:

AMT2105 chip is a high performance high efficiency 7 - 12GHz power amplifier, it is designed based on Gallium Nitrate (GaN) HEMT process, with ground through metal via on the back technology. All chip products are 100% RF tested. AMT2105 is with dual voltage supply, drain voltage Vds = 28V, provides 47.5dBm output power in 7 - 12GHz frequency range.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	35V	
Id	Drain Current	7A	
Vg	Gate Voltage	-1.2V	
lg	Gate Current	150mA	
Pd	DC Power Consumption	196W	
Pin	Input Signal Power	30dBm	
Tch	Operating Temperature	225°C	
Tm	Sintering Temperature	310°C	30s, N₂ protection

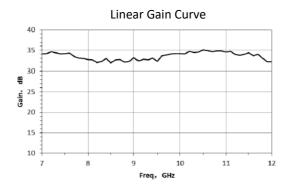
[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

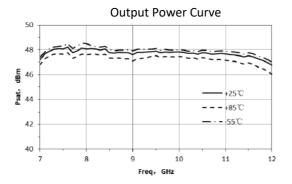
Electrical Characteristics (Ta = 25°C)

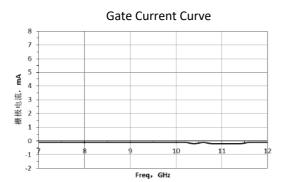
Symbol	Parameter	Test Condition	Value			Unit
			Min	Typical	Max	
Gain	Small Signal Gain		-	33	-	dB
VSWRin	Input SW	Vd = 28V	-	-	2	
Gp	Power Gain	Vg = -2.2V		24		dB
Psat	Saturated Output Power	F: 7~12GHz	-	47.5	-	dBm
PAE	Power Added Efficiency	Duty Cycle: 10%	-	40	-	%
Id	Operating Current		0.4	0.5	0.65	А

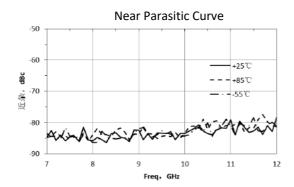
Note, under non-CW operation.

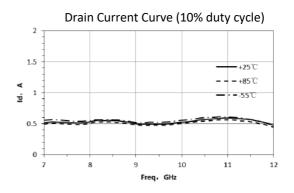
Typical Performance

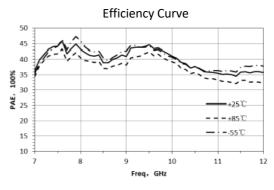


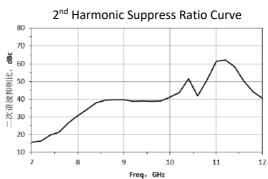


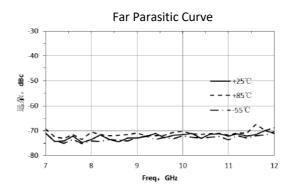




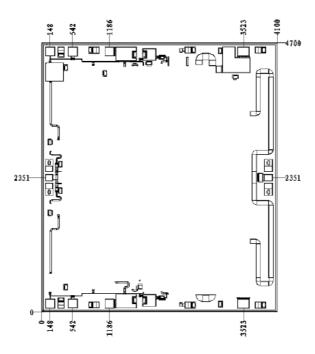




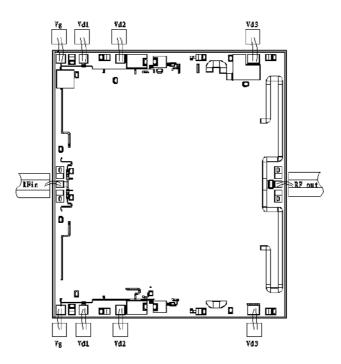




Chip Dimension (Unit: μ m)



Chip Layout Diagram



Pad Definition

Symbol	Function	Dimension	Equivalent Circuit
RF_in	RF signal input port, connecting to external 50Ω system. DC blocking capacitor is needed, if external DC current is applied to this pad.	100*100μm²	RF-in
RF_out	RF signal output port, connecting to external 50 $\!\Omega$ system, no need to add DC blocking capacitor.	100*100μm²	RF_out
Vg	Amplifier gate bias, need external 100pF, 1000pF capacitor.	120*120μm²	Vg of the second
Vd1	Amplifier drain bias, need external 100pF, 1000pF capacitor.	120*120μm²	-P_H-IP Vd1
Vd2	Amplifier drain bias, need external 100pF, 1000pF capacitor.	120*120μm²	Vd2
Vd3	Amplifier drain bias, need external 100pF, 1000pF capacitor.	180*120μm²	-\frac{1}{2}

Please see Appendix A for details.