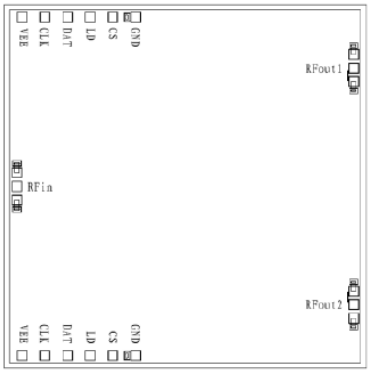
AMT1324

14 - 18GHz Amplitude and Phase Multi-Function Chip



Key Features :

- Frequency range : 14 – 18GHz
- Channel type : dual channel
- Insertion loss : 15dB
- Phase shift bit : 6 bits
- Phase shift step : 5.625°
- Phase shift RMS : 4°, additive attenuation ±0.8dB
- Attenuation bit : 6 bits
- Attenuation step : 0.5dB
- Attenuation RMS : 0.7dB, additive phase shift ±10°
- COM port standing wave : 1.3
- Each channel port standing wave : 1.3
- Operation voltage : -5V
- Control method : two independent channel serial control, control level is compatible with +3.3V and +5V.
- Chip dimensions : 4.0mm x 4.0mm x 0.1mm
- Applications : wireless communication, transceiver module, radio telecommunication etc.

Description :

AMT1324 is a dual channel amplitude and phase multi-function chip, incorporating with power separator, 6-digit control attenuator, 6-digit control phase shifter, 24-digit serial rotate and driver. It is designed by Gallium Arsenide (GaAs) process. The chip typical operation voltage VEE is -5V, with two independent channel serial control, control level is comparable with +3.3V and +5V. This chip is designed with ground through metal vias on the back technology. All chip products p are 100% RF tested.

Absolute Maximum Ratings (Ta = 25°C)

Symbol	Parameter	Value	Remark
VSN	Operation voltage	-4V	
Pin	Max. Input Signal Power	+15dBm	
Tch	Operation Temperature	150°C	
Tm	Sintering Temperature	310°C	30s, N_2 protection
Tstg	Storage Temperature	-65 ~ +150°C	

[1] Operation outside any of the Absolute Maximum Ratings may cause permanent device damage.

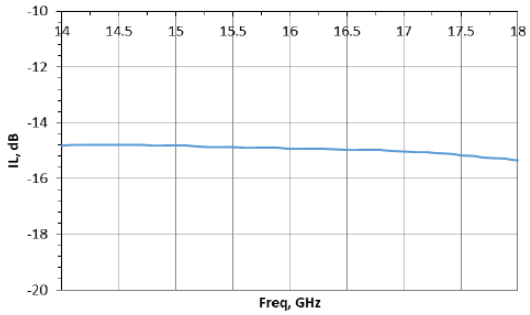
Electrical Characteristics (Ta = 25°C)

Symbol	Parameter		Value			Unit	Remark
			Min	Typical	Max		
F	Frequency			14 ~ 18		GHz	
IL	Insertion loss		-	15	15.5	dB	
PS	Phase shift range			5.625 – 354.375 (6 bits phase shift)		°	
RMS_Pha	Phase shift RMS		-	4	5	°	
Δatt	Phase shift additive attenuation varation	CH1	-	±0.65	±0.75	dB	
		CH2		±0.8	±0.9		
ATT	Attenuation range			0.5 – 15.5 (5 bits attenuation)		dB	
RMS_Att	Attenuation RMS		-	0.7	0.9	dB	
Δpha	Attenuation additive phase shift variation	CH1	-	±7.8	±8.2	°	
		CH2	-	±10	±13		
VSWRin	Input standing wave (attenuation set zero)		-	1.3	1.5	-	
VSWRout	Output standing wave (attenuation set zero)		-	1.3	1.6	-	
VSWRin	Input standing wave (phase shift set zero)		-	1.3	1.5	-	
VSWRout	Output standing wave (phase shift set zero)		-	1.3	1.5	-	

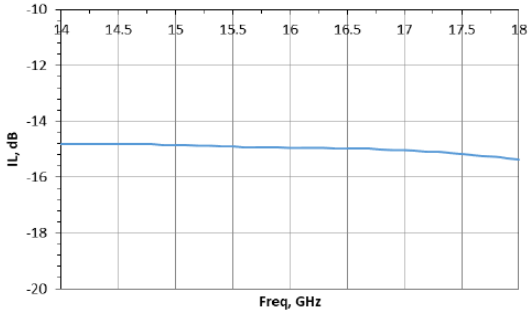
Typical Performance

(1) Insertion Loss

CH1 Phase Shift Attenuation Insertion Loss
(CH2 phase shift attenuation set zero)

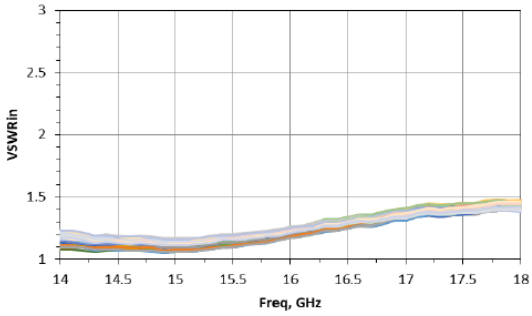


CH2 Phase Shift Attenuation Insertion Loss
(CH1 phase shift attenuation set zero)

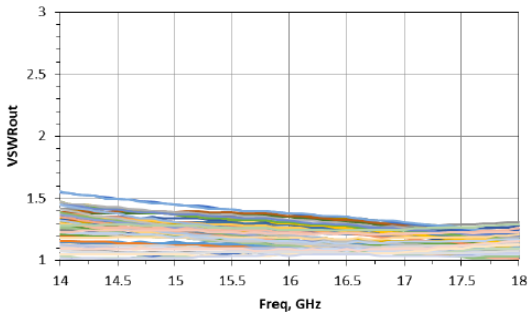


(2) Standing Wave

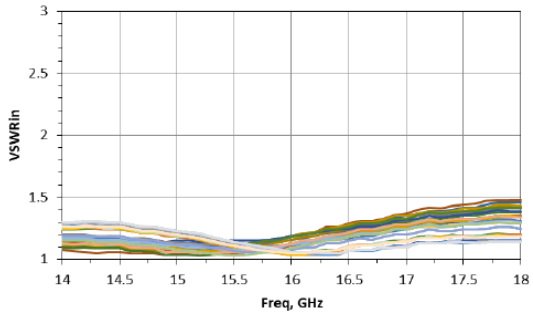
Phase Shift Input Standing Wave
(attenuation set zero)



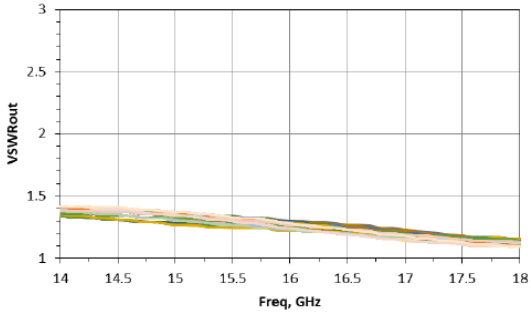
Phase Shift Output Standing Wave
(attenuation set zero)



Attenuation Input Standing Wave
(phase shift set zero)



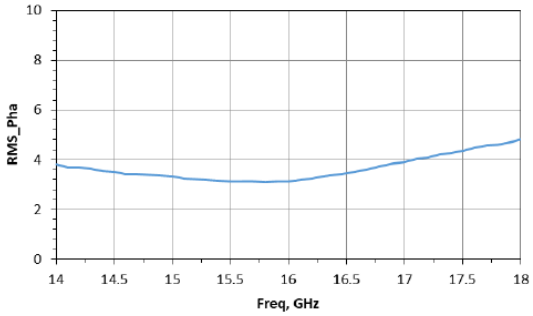
Attenuation Output Standing Wave
(phase shift set zero)



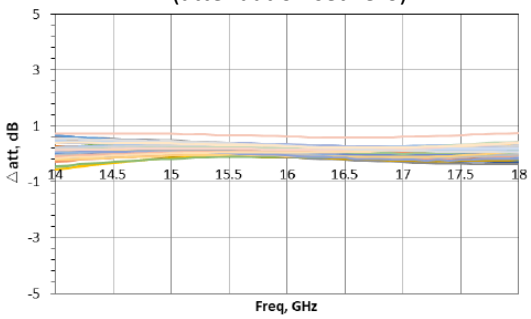
(3) Phase Shift Attenuation

CH2 phase shift attenuation set zero, CH1 phase shift attenuation test results :

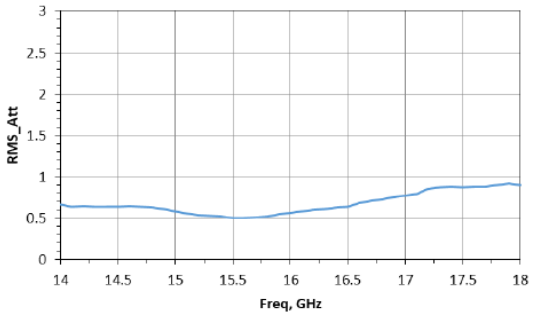
Phase Shift 64 States RMS Error
(attenuation set zero)



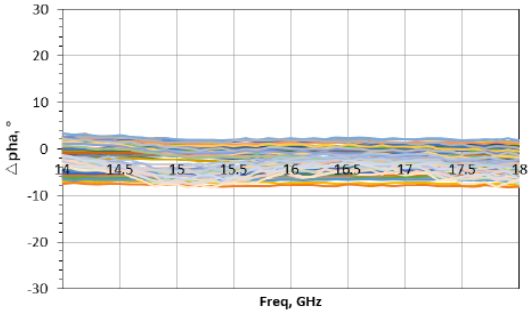
Phase Shift Additive Attenuation
(attenuation set zero)



Attenuation 64 States RMS Error
(phase shift set zero)

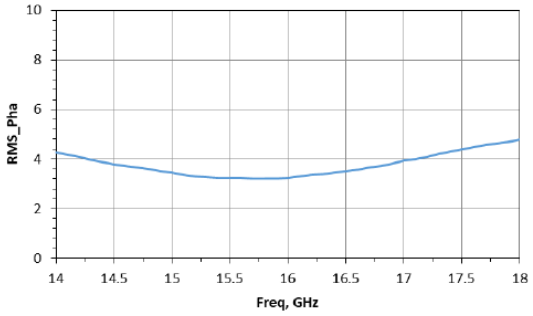


Attenuation Additive Phase Shift
(phase shift set zero)

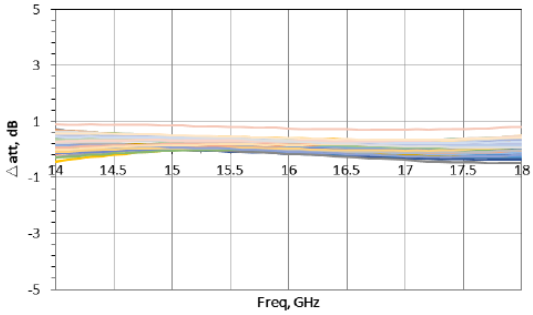


CH1 phase shift attenuation set zero, CH2 phase shift attenuation test results :

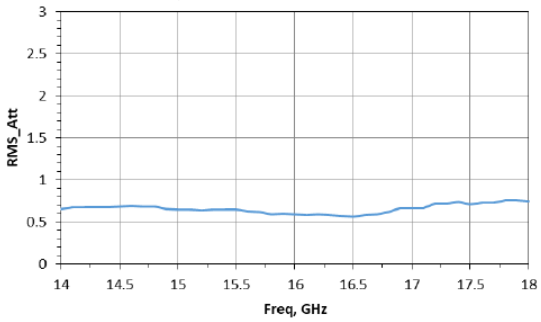
Phase Shift 64 States RMS Error
(attenuation set zero)



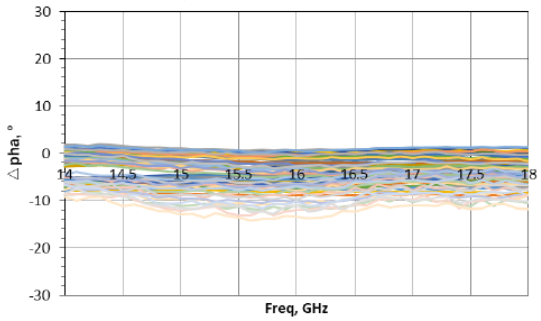
Phase Shift Additive Attenuation
(attenuation set zero)



Attenuation 64 States RMS Error
(phase shift set zero)



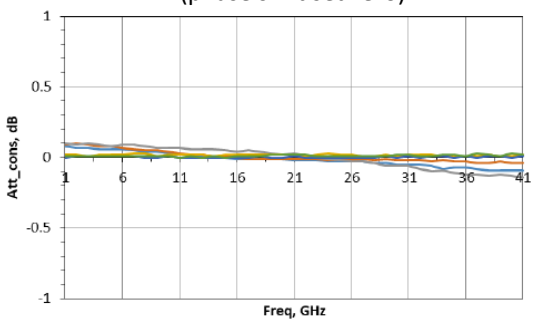
Attenuation Additive Phase Shift
(phase shift set zero)



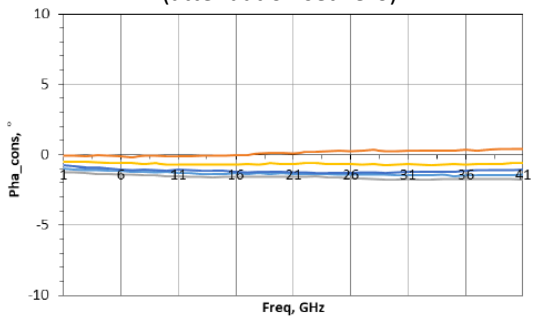
(4) Channel Consistency

Chip Quantity : 5 pcs

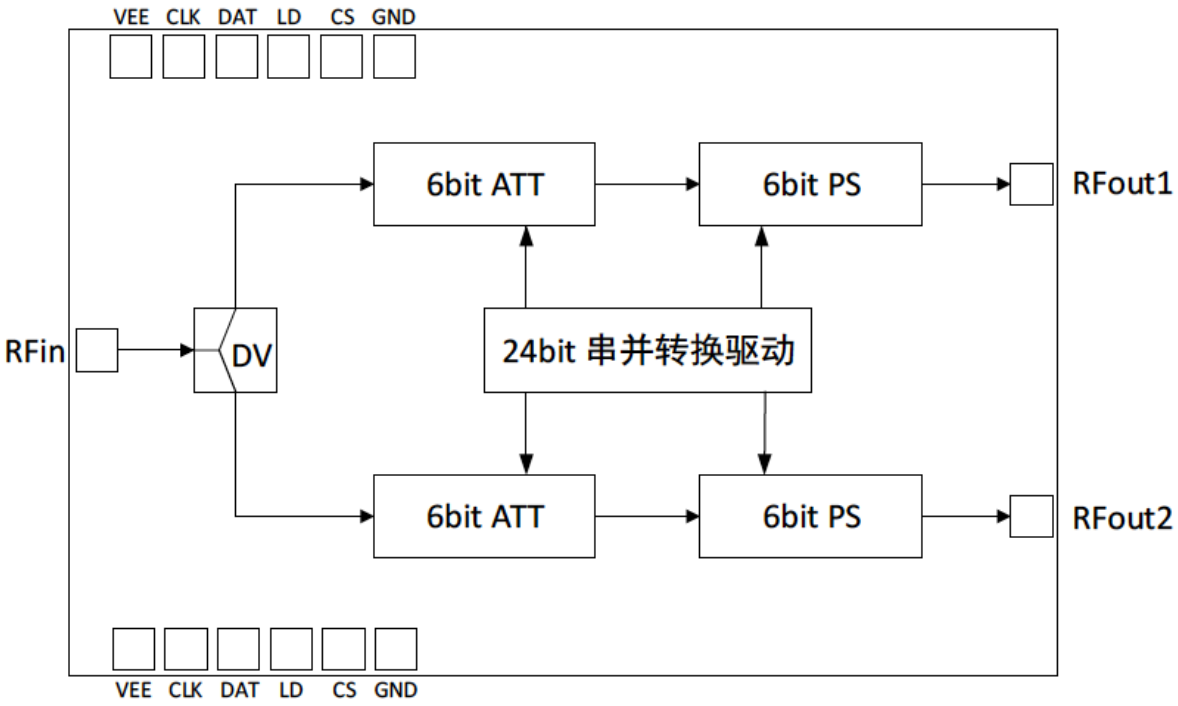
Amplitude Consistency
(phase shift set zero)



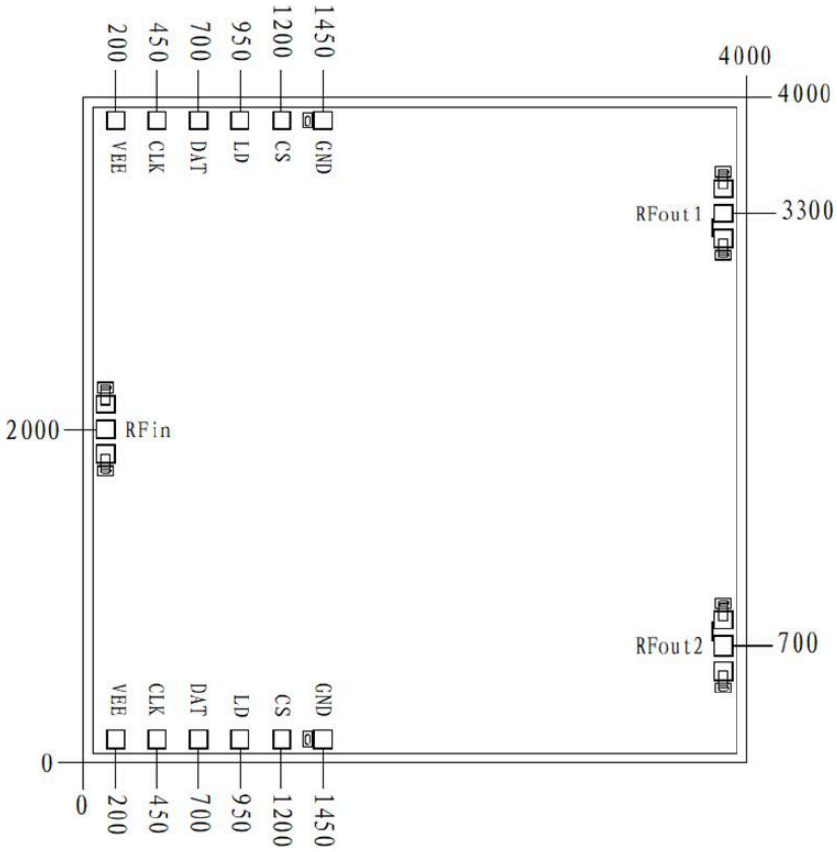
Phase Shift Consistency
(attenuation set zero)



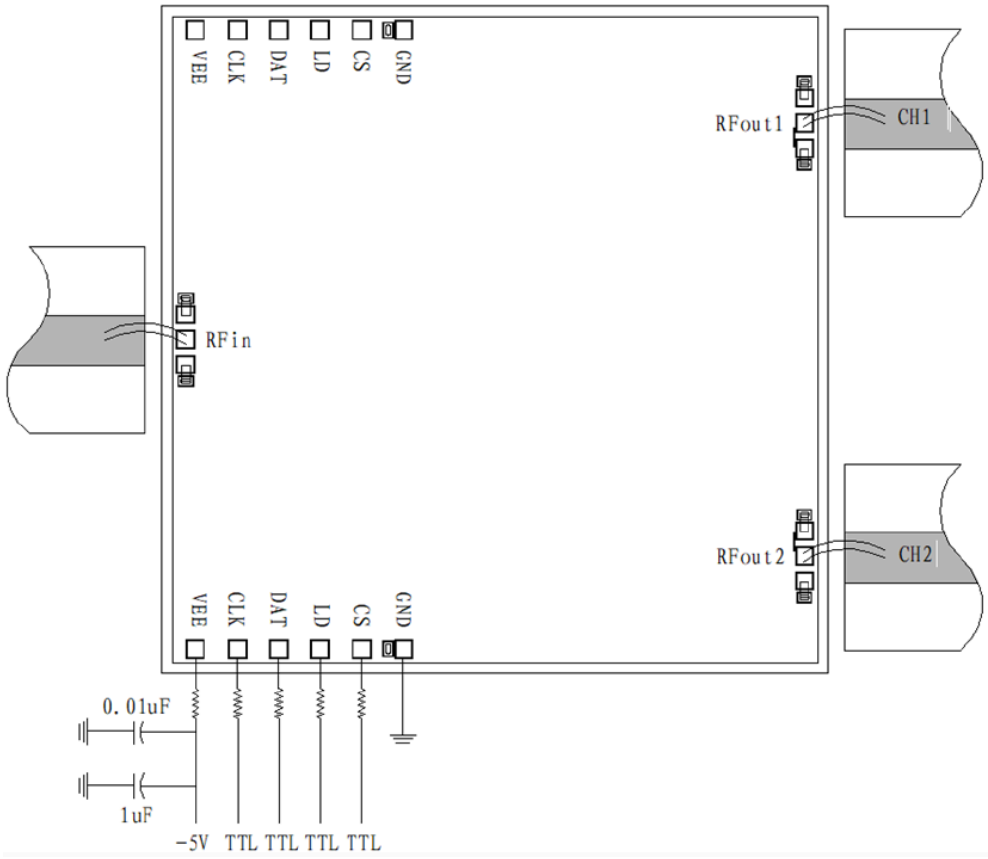
Internal Functional Block Diagram



Chip Dimensions (Unit : μm)



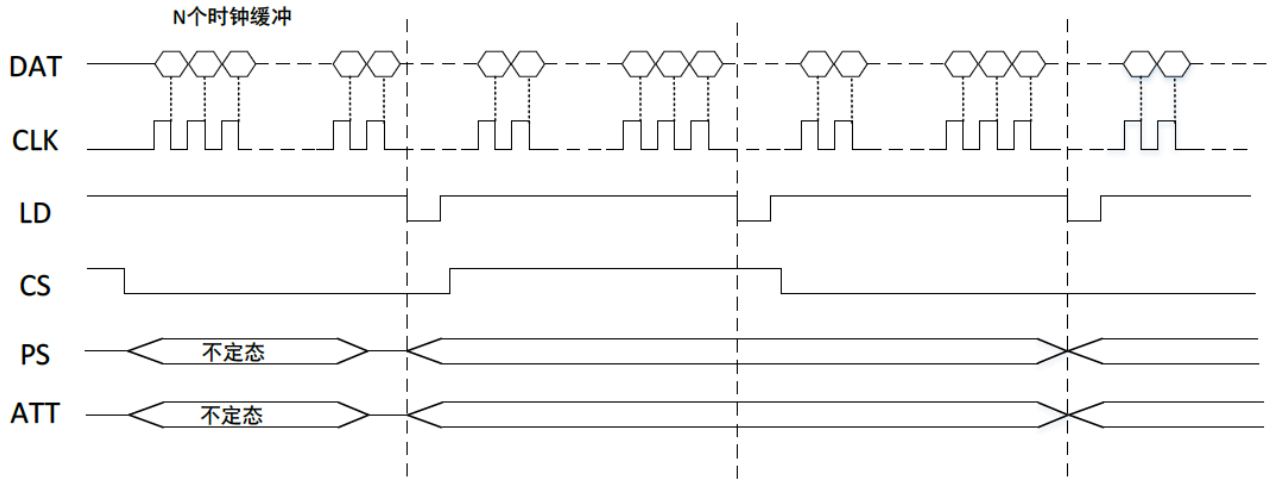
Chip Layout Diagram



Solder Pad Definition

Name	Function Description	Dimension	Explanation
RFin	RF input port	100μm x 100μm	RF input port
RFout1 / RFout2	RF output port	100μm x 100μm	RF output port
VEE	Supply voltage -5V	100μm x 100μm	Supply voltage -5V
CLK	Data clock	100μm x 100μm	Falling edge active
DAT	Data input	100μm x 100μm	24 bits phase shift attenuation control signal
LD	Data latch	100μm x 100μm	Falling edge active
CS	Chip Select	100μm x 100μm	Low level active
GND	Ground	100μm x 100μm	Ground

Timing Diagram



Description :

1) N=24, serial input enable signal CS. Input data DAT, shift clock CLK, latch signal LD are all TTL signal, of which CLK, LD signal are falling edge active, CS signal is low level active;
2) When CS is TTL low level, at CLK falling edge, data is shifted. LD must not be at the CLK falling edge, it latches the serial in data at falling edge after N cycle of CLK. D24 first, D1 last.
3) When CS is TTL high level, the clock signal of wave control circuit is locked, it cannot serial input data, chip retains the data that were previously input.
4) TTL level compatible with 0V/+3.3V and 0V/+5V.

Truth Table

状态		输入串码																						
		D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	D24
零态		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH2 移相衰减(CH1 移相衰减置零)	5.625°	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	11.25°	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	22.5°	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	45°	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	90°	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	180°	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0.5dB	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1dB	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	2dB	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4dB	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8dB	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	16dB	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
CH1 移相衰减(CH2 移相衰减置零)	0.5dB	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	1dB	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	2dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	4dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	8dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	16dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	5.625°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	11.25°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	22.5°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
	45°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	90°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	180°	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Please see Appendix A for details.